DESIGN AND IMPLEMENTATION OF SWITCHED-CAPACITOR FREQUENCY-SELECTIVE FILTERS IN MOS TECHNOLOGY

BY

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A thesis submitted to the Faculty of Science of the University of Edinburgh, for the degree of Doctor of Philosophy.

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February 1983

DECLARATION OF ORIGINALITY

This Thesis, composed entirely by myself, reports on work conducted by myself in the Department of Electrical Engineering at the University of Edinburgh.

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ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my academic supervisor, Professor J Mavor, without whom I would never have reached this stage. Special thanks are also due to Dr J R Jordan for his help and useful discussions.

I am grateful to many friends and colleagues in the Department of Electrical Engineering and Wolfson Microelectronics Institute for their help and useful discussions. In particular, the help of Drs P B Denyer, H M Reekie and J Pennock is sincerely acknowledged.

I am indebted to Professor J O Scanlan and his team at University College Dublin, and also to Dr J Sewell and his colleagues in the University of Hull for their help and support in the early stages of this research.

Financial support from the University of Baluchistan, Zahedan, Iran, in the first two years of this research is acknowledged. I am also grateful to my father, Mr G H Rafat, whose financial support helped me to devote myself to my research.

Last, but not least, I would like to express my sincere appreciation to Mrs Caroline Burns who patiently and carefully typed this thesis.

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To my wife Soraya

CHAPTER 1: INTRODUCTION

1.1 Background to the Research Programme

Electronic, voice-band, frequency-selective filters are an important branch of electric wave filters which potentially serve a wide range of applications in telecommunication and control systems. Voice-band filters (passband < 4kHz) were first realised in the early 1920s, by using discrete, passive components such as resistors (R), inductors (L) and capacitors (C). These filters are known as passive RLC or LC ladder filters and are in widespread use.

Since the size and weight of inductors in RLC filters increase as the passband frequencies decrease, attempts have been made to either integrate them directly in silicon technology or to simulate their behaviour by a combination of other integrable electronic components. Since integrated circuits consist basically of a thin layer, and it is not possible to concentrate sufficient magnetic energy into the thin layer[1], the inductors of required values for voice-band frequencies have so far resisted integration. Therefore the only way to reduce the size and cost of the voice-band filters was to replace them by equivalent networks of other components.

A successful attempt to replace the inductors in passive RLC filters was the introduction of active-RC filters[2], comprised of discrete resistors, capacitors and active devices such as electronic, thermionic valves. Although the active-RC filters offered the possibility of filtering and amplification simultaneously, the major size and cost reduction was only achieved after inexpensive integrated operational amplifiers and thin-film hybrid integrated circuits became available[3].

Despite all advances in integrated technology, the implementation of low cost, fully integrated voice-band active-RC filters was not achieved for many years, either in bipolar or in metal-oxide-semiconductor (MOS) technologies, for the following reasons:

1. Values of resistors and capacitors for audio frequency design are usually too large for integration (typically of the order of mega ohms (MΩ) and thousands of picofarads (pF)).

2. Diffused resistors have poor temperature and linearity coefficients (1500 ppm/^{o}C and 200 ppm/volt respectively)[4].

3. Poor tolerances are obtained in fabricating resistors and capacitors of specific magnitudes. For example, ± 20% of absolute values is typical. Therefore, RC products (time constants) which define the critical frequencies of the active-RC filters will have a large error associated with their definition.

Thus, a modification of active-RC filter topology was necessary, if precision filters were to be efficiently and fully integrated in MOS technology.

The first step towards the implementation of monolithic MOS active-RC filters was taken in 1972, when it was demonstrated[5] that the resistor in simple RC lowpass filters could be simulated

by the combination of a capacitor and two MOS field-effect transistor (MOSFET) switches, controlled by a biphase clock generator. In this rather theoretical study, it was shown that the above mentioned "equivalent resistor" has the value of $R \approx 1/(f_c C_R)$ where f_c is the clock frequency and C_R is the value of the "switched-capacitor". Thus RC time constants can be defined with high accuracy because $RC \approx C/(f_c C_R)$. Further, the ratio of capacitors in MOS integrated circuits can be controlled with a higher degree of accuracy compared to the absolute values of resistors and capacitors. Numerical examples are given below:

1. While the absolute values of MOS resistors and capacitors could have a tolerance as large as ± 10 per cent, the ratio of MOS capacitors can be controlled to 0.1 per cent accuracy[6].

2. The size of the switched-capacitor equivalent resistor decreases as the required resistance value increases. Therefore, the switched-capacitor equivalent resistor requires a very small silicon area to implement large resistance values. For example, to implement a resistance value of 10 MΩ, a capacitor of 1 pF could be switched at 100 kHz rate. This would require a silicon area of approximately $0.01 mm^2$, while for the same value of continuous resistors implemented by using a polysilicon line or diffusion, the area required would be at least 100 times larger[7].

Once again fully-integrated active-RC active filters had to wait for monolithic MOS operational amplifiers until the mid-1970s[8]. Thereafter, several second-order, active, switched-capacitor filters were successfully implemented in MOS technology, by replacing resistors in active-RC filters[9-11]. The reasons for the successful implementation of active switched-capacitor filters are as follows:

1. In contrast to bipolar technology, MOS integrated circuits have the ability of storing charge on a circuit node over a period of many milliseconds and sensing the value of charge continuously and non-destructively. This is because of the high impedance of the MOS transistors in the off state, and the essentially infinite input impedance of MOS transistors in the active mode of operation[7].

2. High density of MOS components, i.e. MOS transistors, capacitors and operational amplifiers.

3. High precision of capacitor ratios, which are used to define filter coefficients.

From a minimum sensitivity point of view, the design of high order switched-capacitor (SC) filters should be based on passive RLC prototypes[12], rather than cascading active second-order (biquad) sections. The first low sensitivity, high-order, SC ladder filters were successfully designed and implemented in MOS technology, during 1978[13-15]. Thereafter, custom designed, monolithic, SC ladder

filters based on established design methods were marketed by Reticon[16]. At this time, research in Edinburgh had just commenced.

The conventional SC second-order and high-order filters were based on an approximate design, i.e. assuming a very high clock rate (very low percentage passband, typically 1-5%). The element values (capacitor ratios) of the SC filters were obtained using the available tables for continuous time, active-RC filters or passive RLC filters. Although using the simplified approximate design, acceptable results for many applications are obtained, but they were not optimum. SC filters are essentially analogue sampled-data systems and so they should be exactly analysed in the z-domain to obtain their optimum filter (transfer function) coefficients.

The major part of this thesis concerns the exact design and subsequent monolithic MOS implementation of a low-sensitivity third-order maximally-flat, all-pole, lowpass, SC ladder filter based on a novel exact analysis method introduced by Scanlan[17]. The above exact design adopted in this thesis is superior to the conventional (approximate) design of SC ladder filters for the following reasons:

1. There is no restriction on the clock frequency, apart from that which is common to all sampled-data systems, i.e. it should be at least twice the highest frequency in the applied signal.

2. The capacitor ratios are obtained optimally and at the same time lower than those obtained from the approximate design.

3. Because the higher passband to clock ratios could be used in the exact design, the useful frequency range of the SC ladder filter extends to higher frequencies.

In the following, the detailed programme of research is presented.

1.2 The Programme of Research

The first objective of the research programme was to design a monolithic MOS integrated MOS lowpass ladder filter based on a novel exact analysis of SC ladder filters[17]. A prototype third-order maximally flat lowpass ladder filter with the cut-off to clock frequency ratio of 12 per cent was designed and implemented in a 5 μm, 15 V polysilicon-gate, NMOS process[18]. This simple filter was selected because it could be treated analytically and therefore helped to illustrate the efficacy of the exact analysis, without the use of involved computing routines. The frequency response of the realised integrated filter was then measured and demonstrated excellent agreement between the theory and experiment (c.f. Chapter 6). Other important measurements were made on these integrated circuit filters such as noise and harmonic distortion.

The second objective was to investigate the use of the conventional bilinear z-transform SC equivalent resistor[19,20] (BER) in deriving SC narrow bandpass (resonator) biquad filters, from the active-RC prototypes. The resulting SC resonators were to be used in a tracking filter topology[21]. During the above investigation, a general approach to the design of SC biquad filters with reduced stray capacitances, was suggested. This part of the

research resulted in an SC tracking filter applied to SC narrow bandpass filters, which is considered as one approach to the future realisation of fully-integrated MOS tracking filters.

1.3 Thesis Format

Chapter 2 gives the theoretical background necessary to understand and design SC filters. A review of published papers on the subject of SC filters and some of their active and inductorless counterparts is also presented.

Design of programmable SC biquad resonators using SC "BER" elements is studied in the first part of Chapter 3. The second part of this Chapter describes one approach to the design of SC tracking filters, as a typical application of the SC narrow bandpass filters (SC resonators).

Chapter 4 is devoted to the theoretical background and a design example relating to the exact design of SC lowpass ladder filters, as well as a comparison with the conventional (approximate) design.

Chapter 5 describes the practical design considerations and the effects of monolithic component imperfections on the overall performance of SC filters.

Chapter 6 presents the NMOS integrated circuit layout of the SC lowpass ladder filter based on the exact analysis and synthesis given in Chapter 4. The experimental results for the above integrated filter are also presented in this Chapter.

Chapter 7 summarises the conclusions of the thesis and suggests some productive extensions to the research work provided herein.

CHAPTER 2: SWITCHED-CAPACITOR (CIRCUIT) FUNDAMENTALS

2.1 Introductory Remarks

Switched-capacitor filters are essentially sampled-data, analogue filters. As a consequence, most of the literature and information available for sampled-data filters is directly applicable to SC filters.

To define the role of SC networks amongst the class of sampled-data systems, we begin with the most general difference equation describing these systems. This is a linear, constant-coefficient, difference equation of the form[22]:

$$y(nT) = \sum_{k=1}^{N} a_k \, y(nT-kT) + \sum_{r=0}^{M} b_r \, x(nT-rT) \qquad (2.1)$$

or in terms of the z operator ($z = e^{j\omega T}$ in the frequency domain):

$$H(z) = \frac{Y(z)}{X(z)} = \frac{\sum_{r=0}^{M} b_r \, z^{-r}}{1 - \sum_{k=1}^{N} a_k z^{-k}} \qquad (2.2)$$

where: $y(nT)$ and $Y(z)$ are outputs of the sampled-data system in time and frequency domains respectively; $x(nT)$ and $X(z)$ are inputs of the sampled-data system in time and frequency domains respectively; b_r are multiplication factors associated with feedforward path of the system; a_k are multiplication factors associated with the feedback path of the system; and, finally, ω and T are frequency (in radian units) and sampling period of the sampled-data system, respectively.

In Eqns (2.1) and (2.2), if the coefficients a_k are all zero, the system will have an impulse response of finite duration and is called FIR (Finite Impulse Response) or the "Transversal" system. Otherwise the system is called IIR (Infinite Impulse Response) or "Recursive". Switched-capacitor filters are IIR filters, because both coefficients a_k and b_k are non-zero, viz: there are both poles and zeros in the system response.

In general, any sampled-data system could be realised by a combination of delay elements (storage elements), adders and multipliers. In the case of SC filters, delay elements are realised by switches and capacitors (Operational amplifiers provide the multiplication and also summation. The implementation aspect will be treated in Chapters 3, 5 and 6.

The present Chapter is divided into two parts. In the first part, the review of the publications on the subject of SC filters and some of their active and inductorless counterparts, is presented. The second part of this Chapter is devoted to the theoretical background necessary to understand and design conventional SC filters.

2.2 Classical Filters

The theory of electrical filters can be traced to 1915, when Wagner and Campbell developed the concept of passive, electric wave filters[23]. Electric wave filters or, briefly, "filters" could be defined as "a network which is required to have a prescribed time or frequency response for a given excitation".

Until the mid 1960s, passive, lumped, LC-filters dominated the field of filters and transmission systems. However, eventually the need for more selective filters caused the exploration of other passive technologies, namely crystal, ceramic, and mechanical filters. Crystal and ceramic filters are those that provide mechanical resonance properties and the capability of energy conversion in one and the same device, while mechanical filters are those which combine two separate materials or devices to perform these functions[3]. Because, during the last two decades, great size and cost reductions have been achieved with crystal and mechanical technologies, they are still in widespread use, but their main disadvantage is that they could only be used as bandpass or bandreject filters[24].

A second approach to the development of inductorless filters is RC-active filters which make use of linear amplifiers (active elements) and passive resistors and capacitors[25]. One of the most important advantages of this branch of filters is that they lend themselves to advanced hybrid and MOS technologies, and hence are fully integrable in a single silicon chip. In Chapter 3, active RC-filters are the starting point for deriving SC filters.

As far as analogue inductorless filters are concerned, for low-to-medium pole Q's (5-20) at low-to-very low frequencies (20 kHz-0.1 Hz), no alternative to active-RC filters exists. Also in the voice frequency band, where functional versatility (flexibility in frequency range) is an important consideration, again there is no viable alternative to active-RC filters[3]. Among the advantages of RC active filters are small size and weight, simplicity of synthesis and tuning, isolation of stages, and large available gain.

2.3 Switched Networks

Switched circuits as a general rule (i.e. circuits composed of linear constant elements and periodically-operated switches) have played a major role in communication engineering since the late 1930's[26]. Among those who have contributed to the theoretical development of early switched filters is Fettweis[27], who still is a major contributor to the field of modern switched-capacitor filters. The first results obtained in relation to Fettweis' theoretical ideas which were based on the so-called resonant-transfer principle, were presented by Boite and Thiran in 1968[28].

Later development on periodically-switched filters led to a large number of papers[29] on the analysis generally of such filters. Among these, Sun and Frisch[29] have pointed out that the effective values of resistors can be increased by time-switching. The time-constant of the circuit is a function of both the duty cycle and the switching frequency. Thus for precise timing, both have to be accurately controlled. Liou[30] has given an exact analysis for periodically-operated switches. Hirano and Nishimura[31] have extended the concept to active-RC filters. They have demonstrated

that multiplication of resistances and multiplication of gyration conductances in an active-RC network, and multiplication of transfer coefficients of controlled sources and negative impedance converters can be achieved by means of the switching techniques.

Another attempt to build inductorless filters by making use of switches and capacitors resulted in a class of switched filters called N-path filters[23]. A drawback of N-path filters and early switched-capacitor filters in general is that because of the modulation process, they are not direct substitutes for conventional LC filters[1]. Also their application is limited to only bandpass filters.

2.4 Sampled-Data Analogue Filters

2.4.1 Charge Transfer Devices (CTD's)

Charge-transfer devices, including the important branch of Charge-Coupled Devices (CCD's), were the first filters which efficiently utilised the charge storage property of MOS technology[32]. Although CCD transversal filters are powerful filters in certain applications such as adaptive and matched filtering[33], in the applications with which this thesis is concerned, they are inferior to recursive SC filters. For example, they can only realise zeros and not poles (transversal), and the resulting high insertion loss (typically -20dB) of the filter, limits the output dynamic range. A comparison between SC filters and CCD's[34], shows that as far as coefficient accuracy, noise and dynamic range, operational amplifier quality requirements, and process sensitivity are concerned, SC filters are superior to CCD's in certain applications. However, there is no doubt that CCD filters will be applied to electronic systems for many years to come.

2.4.2 Switched-Capacitor Filters

The first monolithic recursive filters using switched-capacitor techniques have been implemented using direct-form second-order digital filter section[35,36], rather than replacing resistors in active-RC filters. The main disadvantage of this approach is the increased sensitivity of the filter to its coefficient values as the ratio of the sampling rate to passband frequencies is increased.

It seems that active-RC filters have long been waiting for MOS technology. Although they have already been integrated[3] using hybrid technology, which was a suitable solution to replace discrete resistors, capacitors and electronic tubes, and also for relatively economical large-quantity production, but because integrated resistors had poor temperature and linearity coefficients, RC products and hence the passband edge of filters, could not be defined accurately. Moreover, they occupied a large area of the circuit. It was Fried[5] who first replaced resistors in a simple passive-RC filter by a capacitor and two MOS FET switches. Therefore, the frequency characteristics of the new proposed filters were not dependent on RC products but rather on capacitor ratios and two synchronised non-overlapping clocks which could be controlled to a high degree of accuracy.

Although Fried had, in 1971, pointed out the possibility of using MOS technology to realise SC filters, the first MOS SC filters were not realised until 1977 when Hosticka et al[9, 10] and Caves et al[11] presented their first experimental results.

The principle of the first SC equivalent resistor which is now

known as the parallel SC equivalent resistor (PER) is shown in Fig. 2.1. In this figure switches S_1 and S_2 are MOS transistors whose gates are controlled by a biphase non-overlapping clock, as shown in Fig. 2.1(d). Therefore, only one of them is closed at one instant. Now suppose the left MOS switch is closed first, then capacitor C_R is charged to the voltage V_1. In the next instant when the clocks have changed their phases, the second MOS switch (right) is closed, and the capacitor C_R is discharged to the voltage V_2. The amount of charge which flows into (or from) V_2 is thus $Q = C_R (V_2 - V_1)$. If the switches are closed and opened at a rate of f_c, then the average current flow i from V_1 to V_2 will be $C_R (V_2 - V_1) f_c$ where $f_c = \frac{1}{T}$, T being clock period. Thus the size of an equivalent resistor which conducts the same package of charge per unit time (average current) as this circuit is:

$$R_{eq} \approx \frac{1}{f_c C_R} \tag{2.3}$$

assuming that the MOSFETs are ideal and the clock frequency is too high.

The above relationship shows the higher the value of R the lower the capacitor C_R in the SC filter, which is a great advantage in low frequency filtering.

The advent of switched capacitor filters is so important that it was once called: 'A revolution in low frequency filtering'[37], and it has so attracted the attention of filter designers and circuit theoreticians that since 1978, within three years, over two hundred papers have been published in different languages, about the analysis,

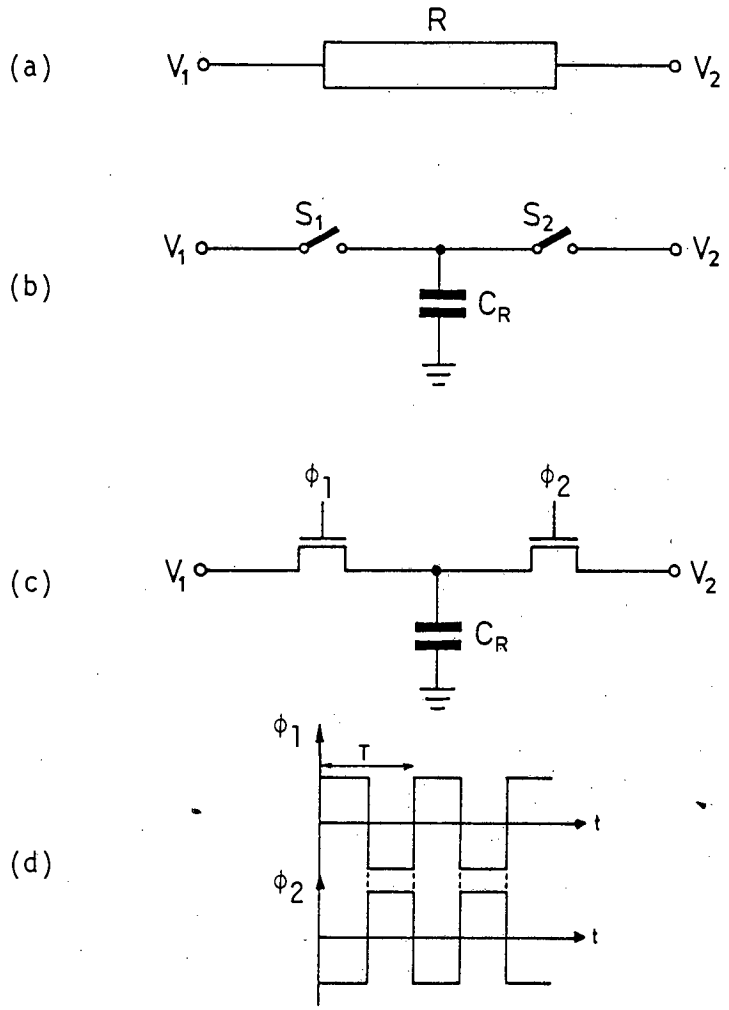


FIG.2.1: Principle of the switched-capacitor equivalent resistors:

(a) A resistor.

(b) A switched-capacitor equivalent of (a), using a capacitor and two ideal switches S_1 and S_2.

(c) As in (b), but using two MOS transistor switches controlled by two non-overlapping clock pulses ϕ_1 and ϕ_2, shown in (d).

(d) Non-overlapping clock pulses ϕ_1 and ϕ_2.

design, and application of SC filters[212,213]. They have already been used in telecommunications [38-58], and they are now at the stage of being used[59] in consumer electronics in the Japanese electronics industry.

Most of the present switched-capacitor circuits are based on resistor replacement, originally suggested by Fried. Fried had outlined the possibility of using MOS technology in realising integrated RC filters, but the lack of fully integrated MOS operational amplifiers, prevented the realisation of fully integrated MOS active-RC recursive precision filters. In late 1977, Hosticka et al introduced the first fully integrated state-variable biquad filter section using NMOS technology. About the same time, Caves et al independently investigated the possibility of replacing resistors by switched-capacitor elements, both in passive-RC and active-RC second-order filters and outlined the practical limitations using polysilicon-gate NMOS technology. In addition to the conventional 'parallel SC equivalent resistors' (PER), Caves et al introduced another SC configuration called 'Series SC equivalent resistor' (SER). The above two different SC equivalent resistors are shown in Fig. 2.2 and their differences are discussed in some detail in section 2.5.1 and 2.5.2.

During 1978 two major improvements in the design of the SC filter were introduced. The first was SC ladder filters simulating active ladder or leap-frog filters, introduced by Allstot et al in the ISSCC-78 Conference[13]; and the second one was a new SC equivalent resistor, namely 'the bilinear SC equivalent resistor' (BER II) proposed by Temes et al[19,20,60-63]. Later Rahim et al introduced another version

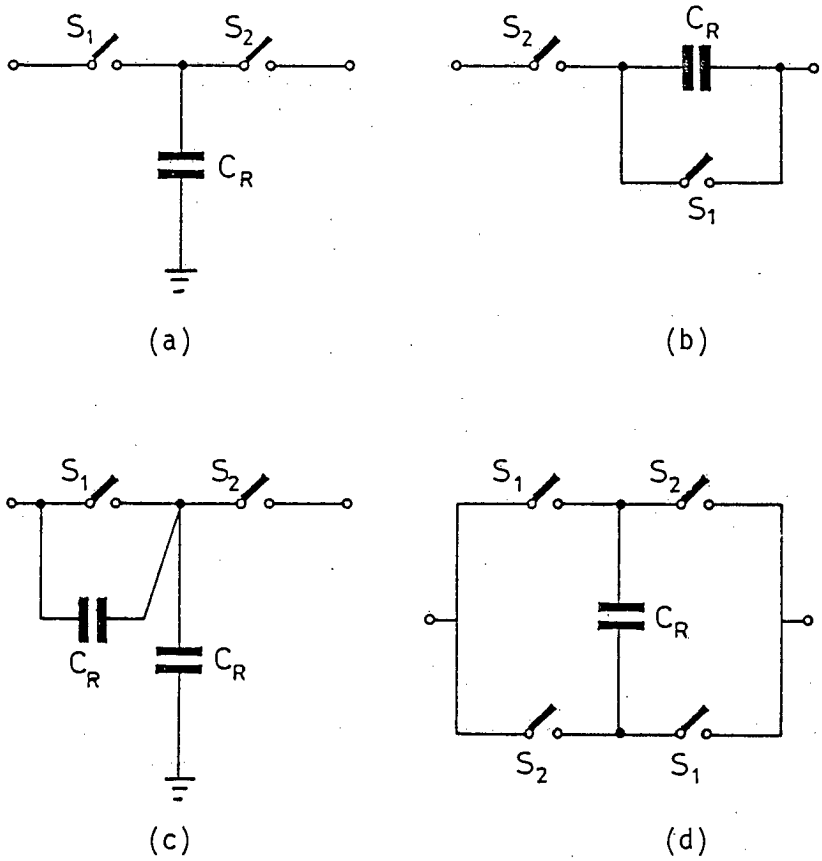


FIG.2.2: Different types of switched-capacitor equivalent resistors:

(a) Parallel equivalent resistor (PER).

(b) Series equivalent resistor (SER).

(c) Bilinear equivalent resistor I (BER I)-(Rahim).

(d) Bilinear equivalent resistor II (BER II)-(Temes).

of the BER element[44], which is inferior to the one introduced by Temes, because of additional capacitor and sensitivity of the circuit to capacitor mismatch. Both versions are shown in Fig. 2.2 and their advantages over the previous PER and SER elements will be discussed in section 2.5.3.

The above two improvements in SC filter design formed the basis for the most recent advances in SC filter design. The major part of the present thesis is devoted to the practical realisation of a novel design method for SC ladder lowpass filters and an examination of the practical limitations of SC's in biquad filters employing BER elements.

SC ladder filters which were based on active ladder filters and enjoyed the very low sensitivity of classical RLC passive filters, soon attracted the attention of industry so that in early 1979, they were already marketed by Reticon[16]. At this time, research in Edinburgh had just commenced. This fact illustrates the extent of the difficulties experienced in contributing to the fast developing field of SC filters. Fortunately, it was found that, despite the ingenious circuit configurations of early SC ladder filters, they suffered from many assumptions and limitations, e.g. high clock to passband ratios and very limited passband (1-5%). Through collaborative research at Edinburgh University and University College Dublin for the first time SC lowpass ladder filters were designed and demonstrated in which these restrictions could be removed (1981). The new improved design method which gives practical and theoretical advantages, forms the content of Chapters 4 and 6.

At this point, it is appropriate to point out the other approaches to the design of SC ladder filters based on passive RLC filters. Apart from the works in Berkeley[14] and in Edinburgh[18], and a more recent publication by Martin et al[65], and Davis et al[66], which are based on operational simulation of RLC ladder filters, most of the recent research on ladder filters is based on element by element replacement of passive RLC filters. Following this approach many papers have been published during 1979 in relation to SC simulation of grounded and floating inductors[67-73]. Among those who have contributed to the design of SC ladder filters is Lee, who has published papers on stray-insensitive and bilinear SC ladder filters[74-79]. Although a part of his early attempts was to overcome the practical problems associated with conventional SC ladder filters, in so doing he ended with a more complicated circuit using many extra switches and capacitors.

Fettweis who has contributed to electronic filters since the 1950's, now has his own place in SC filter design[80-83]. His SC filters are based on low-sensitivity RLC passive filters, and use of the established resonant-transfer principle[23], as well as element by element replacement in SC filters. The main problem associated with his circuits, is the presence of many floating nodes which make the circuit sensitive to stray capacitances.

At this point it is worth mentioning that other research on SC realisation of filters has been undertaken in Edinburgh by Reekie[84] concurrent with this thesis which is very interesting for the following reasons: it is based on low sensitivity RLC passive filters; it uses bilinear z-transformation; and most importantly it

uses only unit-gain buffers which are easier to design and smaller compared to operational amplifiers. Against the many advantages mentioned above, these circuits suffer from almost the same problems associated with Fettweis' SC realisation mentioned previously. Also in conventional SC filters some attempts in designing filters with unit-gain buffers in place of operational amplifiers have been made[85-89]. These filters are complicated in design and so far only simple second-order sections have been realised on the basis of the proposed principles[87-88].

Since the trimming of MOS SC filters after they have been implemented in integrated circuit form is difficult and time consuming, and moreover the accurate prediction of stray-capacitances is difficult because of the process variation, it is always desirable to have a design which is insensitive to parasitics including stray capacitances. In relation to this subject, many circuit designers have attempted to introduce stray insensitive SC filter designs[90-110]. The leaders of this group are Martin et al, and Fleischer et al, who have independently extended their ideas to more general circuits. Presently, almost all circuit designers try to design stray insensitive SC circuits. The first part of Chapter 3 in the present thesis shows one way of designing insensitive state-variable biquad filters derived from the systematic development of bilinear z-transform SC element (BER).

Another distinct approach to designing sampled-data filters is that in which neither operational amplifiers, nor unit-gain buffers are used[111-114]. Although they have the advantage of consuming less area and d.c. static power, their experimental results have not reached farther than realising a simple integrator.

N-path filters which have been in use for narrow band filtering for a long time, are now gaining the advantages of SC filters and MOS technology. In this connection, a number of papers have been published[115-121]. The main disadvantage of SC n-path filters is their limited application to bandpass filtering.

In parallel to research on synthesis and design of SC filters, theoretical studies on SC filter analysis were carried on with the aim of providing related computer programmes. The first result of this attempt was reflected in an excellent paper by Kurth and Moschytz[122-123], which formed the basis of most present computer programmes for SC filters. Soon after them, Laker[124] extended their library of building blocks to include SC elements comprised of one capacitor and from one to four switches which provided a means to derive canonic z-domain equivalent circuits for any SC network. Then Tsividis proposed an exact design of SC networks with cisoidal input[125-126] as an improvement to the early papers which had assumed sampled inputs. Lio and Kuo introduced an exact analysis method which had none of the constraints associated with the previous analytical methods, i.e. exact analysis of SC circuits with arbitrary inputs including cisoidal, sample-and-hold, and noise without topological and duty cycle constraints imposed on the circuits[127-128]. Kurth and Moschytz extended their previous ideas independently, which resulted in a computer programme called SCANAL[129-131] and an improved analysis method which provided similar results as those which Lio and Kou had obtained by a different approach[132]. Simplified analysis methods of SC circuits have also been reported[133-137].

Among the computer programmes proposed for SC network analysis,

perhaps DIANA-SC introduced by De Man et al [138] is the most powerful as it facilitates a general and complete method for the time and frequency domain analysis, including all possible effects, e.g. aliasing, resistive effects, operational amplifier poles, as well as sensitivity and noise analysis. Recently, most universities and electronics companies are developing their own computer programmes. These SC network analysis programmes include SCNAP[139-141], SCAP[142], and SCOP[143]. The SCNAP programme is now being used in Edinburgh. In Appendix A a brief description of the SCNAP programme with its advantages and disadvantages is given.

2.5 Frequency Transformation from s to z Domain

As a member of the sampled-data filter group, SC filters can benefit from the standard design methods described in the literature[144-145]. For example, using continuous time transfer functions to obtain the sampled-data counterparts is a well-known method in the digital and sampled-data field. Although the above method may be employed in obtaining SC filter transfer functions for practical realisations, SC filter topologies are obtained much more directly than other sampled-data filters; as the former could be simply obtained by replacing resistors in active or passive RC filters, by SC elements shown in Figure 2.2. This is one of the advantages of SC filters.

The reasons for employing continuous time transfer functions and analogue circuit topologies are as follows[145].

1. The art of analogue filter design is highly advanced, and since significant results can be achieved, it is

advantageous to utilise the design procedures already developed for analogue filters.

2. Many useful analogue design methods have relatively simple closed-form design formulae. Therefore, sampled-data filter design methods based on such analogue design formulae are rather simple to implement.

3. In many applications it is of interest to use a sampled-data filter to simulate the performance of an analogue (linear time-invariant) filter.

The four widely used general procedures for obtaining sampled-data transfer functions from their analogue counterparts are: difference transformations, bilinear transformation, impulse invariant transformation, and matched z-transformation techniques. In the following sections only two methods, namely mapping of differentials and bilinear transformation, which are most popular in SC filter design, will be explained. To the best of our knowledge, the other two methods have never been used in designing SC filters.

There are other, less general transformations, namely DDI (Direct Discrete Integrator) and LDI (Lossless Discrete Integrator) transformations, which are particularly used in SC ladder filter design. These types of transformations are employed to transform continuous-time integrators to sampled-data integrators and will be described in Chapter 4, where SC lowpass ladder filter design is explained.

2.5.1 Forward Difference Transformation: Switched-Capacitor "PER" Elements

The Forward Difference Transformation (FDT) is a technique[144] which is employed to replace differentials in continous time system equations by finite differences of the following form:

$$\frac{dy}{dt} \approx \frac{y(n+1) - y(n)}{T} \quad \text{when T is small} \tag{2.4}$$

which in terms of the Laplace operator s and sampled-data z operators corresponds to:

$$s \equiv \frac{z - 1}{T} \tag{2.5}$$

or

$$z \equiv 1 + sT \tag{2.6}$$

In SC filters, the above transformation from continuous time viz s-domain to discrete time viz z-domain is performed by replacing resistors in passive or active-RC filters. In the case of forward differences, all resistors in the RC filter are replaced by parallel equivalent resistor (PER) shown in Fig. 2.2(a), first introduced by Fried[5]. Through the above simple resistor replacement, a continuous time active or passive RC filter is transformed to a sampled-data analogue SC filter, and the related transfer function could simply be obtained by using replacements defined in Eqns (2.4) or (2.5).

In any transformation (mapping) from continuous to discrete space, it is desirable that[145]:

(a) The $j\Omega$ axis in the s-plane be mapped to the unit circle in the z-plane, and

(b) points in the left-half s-plane (Re [s] < 0) be mapped inside the unit circle ($|z| < 1$).

Property (a) preserves the frequency selective properties of the continuous system, whereas property (b) ensures that stable, continuous systems (filters) are mapped into stable discrete systems.

To investigate property (a) for forward differences or equivalently PER elements, we start from Eqn (2.6). When $s = j\Omega$, we obtain

$$z = 1 + j\Omega \tag{2.7}$$

The contours in the s-plane and z-plane for this mapping are shown in Fig. 2.3(a). As it is evident from this figure and Eqn (2.7) property (a) of the mapping is not satisfied.

To see whether property (b) of the mapping is satisfied, we set:

$$sT = \alpha + j\beta \tag{2.8}$$

where α and β are real and $\alpha < 0$. Then Eqn (2.6) shows:

$$z = 1 + \alpha + j\beta \tag{2.9}$$

or $$|z| = ((1+\alpha)^2 + \beta^2)^{\frac{1}{2}} > 1$$

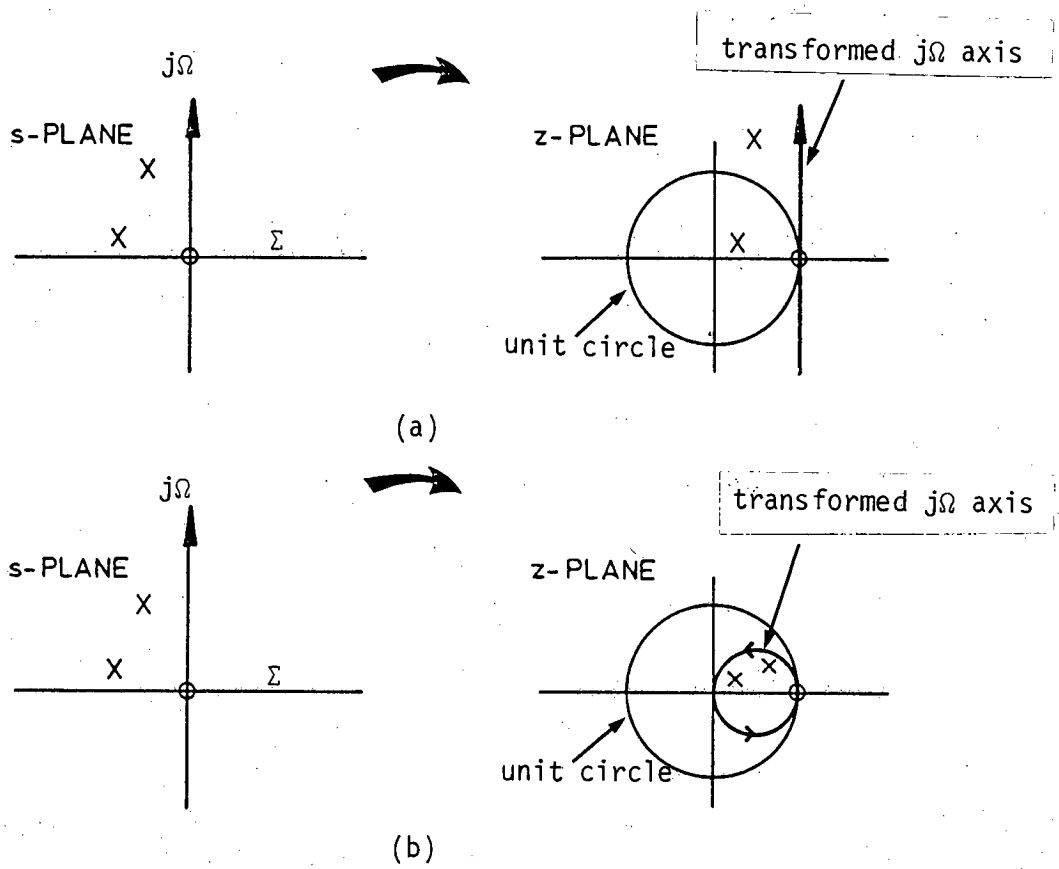


FIG.2.3: Mapping of the jΩ axis and the left-half poles and zeros from s-plane to z-plane, using the forward difference transformation (a), and the backward difference transformation (b).

when $\beta^2 > 1 - (1 + \alpha)^2$.

Therefore property (b) of the mapping is not "in general" satisfied either.

Now it may be argued that the use of the forward difference method or alternatively the PER element to obtain the SC filter from the continuous counterpart is questionable, if the resulting circuit does not preserve the frequency characteristics and stability of the original continuous time filter. An immediate answer is that replacing resistors in RC filters by PER elements provides an easy and suitable means to obtain an SC filter topology. Then from Eqns (2.5) to (2.7) it is evident that if ΩT $(= \frac{\Omega}{f_c})$ is small enough or in other words if the sampling or clock frequency f_c is high enough compared to the frequency of interest Ω, then satisfactory results could be obtained. On the other hand, if one is not satisfied with the resulting approximate transfer function, the proper approach is to analyse the SC circuit resulting from resistor replacement (by PER or any other element), rather than using the simple algebraic substitution of Eqn (2.5).

2.5.2 Backward Difference Transformation: Switched-Capacitor "SER" Element

Another approach to obtain discrete difference equations from continuous differential equations is one for which the following replacement is performed[144]:

$$\frac{dy}{dt} \approx \frac{y(n) - y(n-1)}{T} \qquad (2.10)$$

The above finite difference is known as the Backward Difference Transformation (BDF). Eqn (2.10) may be written in the following form:

$$s \equiv \frac{1 - z^{-1}}{T} \tag{2.11}$$

or

$$z \equiv \frac{1}{1 - sT} \tag{2.12}$$

In SC filters the above transformation is realised by replacing resistors in passive or active-RC filters by an SC element known as series SC Equivalent Resistor or briefly "SER" element, shown in Fig. 2.2(b), which was first introduced by Caves et al[11].

To examine properties (a) and (b) defined in the previous section which are known as frequency characteristics and stability properties for backward difference transformation, we may proceed in the following order[144]:

Using the substitution $s = j\Omega$ in Eqn (2.12), we obtain:

$$z = \frac{1}{1 - j\Omega T} = \tfrac{1}{2}\left(1 + \frac{1 + j\Omega T}{1 - j\Omega T}\right)$$

$$= \tfrac{1}{2}\left(1 + e^{2j\tan^{-1}\Omega T}\right) \tag{2.13}$$

Taking real and imaginary parts of z results in:

$$\mathrm{Re}\,[z] = \tfrac{1}{2} + \frac{\cos\,(2\tan^{-1}\Omega T)}{2}$$

$$\text{Im}[z] = \frac{\sin(2\tan^{-1}\Omega T)}{2} \tag{2.14}$$

Thus mapping of the line $s = j\Omega$ (from $\Omega = -\infty$ to ∞) in the z-plane is the circle described by:

$$\{\text{Re}[z] - \tfrac{1}{2}\}^2 + \text{Im}[z]^2 = (\tfrac{1}{2})^2 \tag{2.15}$$

i.e. a circle with centre at $\text{Re}[z] = \frac{1}{2}$ and radius $\frac{1}{2}$, as shown in Fig. 2.3(b). According to Eqn (2.13) and Fig. 2.3(b), except for extremely small values of ΩT, the image of the $j\Omega$ axis in the s-plane is off the unit circle in the z-plane. Therefore property (a) is not in general satisfied.

To see whether property (b) of the mapping is satisfied, we replace sT in Eqn (2.12) by Eqn (2.8) defined in the previous section, which results in:

$$z = \frac{1}{1 - \alpha - j\beta} \tag{2.16}$$

or

$$|z| = \frac{1}{((1 - \alpha)^2 + \beta^2)^{\frac{1}{2}}} \quad , \alpha < 0 \tag{2.17}$$

Therefore, the stable analogue filter maps into a stable sampled-data SC filter using backward differences which is equivalent to replacing the resistors in RC filters by SER elements. Note that the frequency selective properties are not maintained by the above replacement, except for very high sampling frequency f_c compared to the frequency of interest.

The argument about the reason and extent of usages developed for the PER element in section 2.5.1 is equally valid for the SER element.

2.5.3 Bilinear Transformation: Switched-Capacitor "BER" Element

The most widely used transformation used in designing digital and sampled-data filters is the Bilinear Transformation (BT). This transformation, which is a simple conformal mapping from the s-plane to the z-plane, is defined by the following relation[145]:

$$s \equiv \frac{2}{T}\frac{(1 - z^{-1})}{(1 + z^{-1})} \tag{2.18}$$

In switched-capacitor filters, replacing resistors in RC active filters, by "BER" SC structures shown in Fig. 2.2(c) and (d), provides the desirable transformation defined in Eqn (2.18)[20]. This replacement has a double advantage: it provides the circuit topology of sampled-data SC filters; and at the same time the SC filter transfer function may be analytically obtained by a simple replacement of Eqn (2.18). In other words:

$$H(z) = H(s)\Big|_{s = (\frac{2}{T})[(1 - z^{-1})/(1 + z^{-1})]} \tag{2.19}$$

To examine the validity of this transformation in relation to selectivity and sensitivity properties mentioned in the last two sections, we may solve Eqn (2.18) for z in terms of s.

Thus

$$z = \frac{(2/T) + s}{(2/T) - s} \tag{2.20}$$

which after replacing s by $j\Omega$, results in

$$z = \frac{(2/T) + j\Omega}{(2/T) - j\Omega} \tag{2.21}$$

From Eqn (2.21) it may be concluded that: firstly $|z| = 1$; secondly, $z = 1$ for $\Omega = 0$; and, finally, $z = -1$ for $\Omega = \infty$. Therefore, the entire imaginary axis in the s-plane is mapped onto the unit circle in the z-plane via bilinear transformation, as shown in Figure 2.4(a). Thus selectivity property is now preserved. But at the same time a nonlinear relationship between analogue frequency Ω and sampled-data frequency ω (warping), is introduced. To demonstrate this nonlinearity, Eqn (2.18) could be employed. After substituting for $z = e^{j\omega T}$ and $s = j\Omega$, we obtain:

$$j\Omega = \frac{2}{T} \frac{(1 - e^{-j\omega T})}{(1 + e^{-j\omega T})} \tag{2.22}$$

or by using trigonometric identities:

$$j\Omega = \frac{2}{T} \frac{[e^{j(\omega T/2)} - e^{-j(\omega T/2)}]}{[e^{j(\omega T/2)} + e^{-j(\omega T/2)}]}$$

which results in the following relation:

$$\Omega = \frac{2}{T} \tan(\omega T/2) \tag{2.23}$$

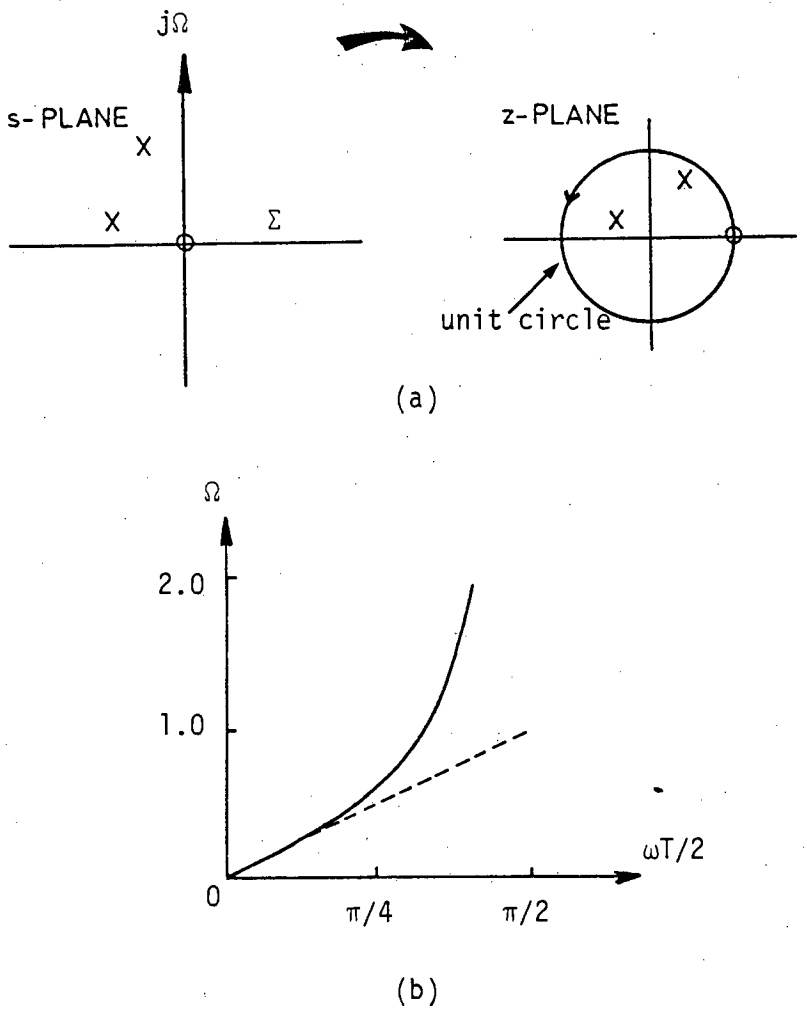


FIG.2.4: s-plane to z-plane transformation (a), and the non-linear warping effect (b) of the bilinear transformation.

This nonlinearity is shown in Fig.2.4(b)[145]. As it may be verified from Eqn (2.23), and also Figure 2.4(b), for small values of ω compared to sampling frequency $f_c = \frac{1}{T}$, the mapping is almost linear. For higher frequencies, Eqn (2.23) may be used for prewarping the desired frequencies such as 3 dB-cutoff or centre frequencies, etc. The prewarping method is employed in the next chapter where the bilinear transformation is used for designing SC filters.

Although the warping aspect of bilinear transformation restricts its application to piece-wise constant continuous systems[144] including lowpass, bandpass and bandstop filters, at the same time this technique sharpens the attenuation regions of these filters, which is regarded as a desirable advantage.

Now to verify the stability property of bilinear transformation, we may set $s = \Sigma + j\Omega$ in Eqn (2.20) to obtain:

$$z = \frac{(2/T) + \Sigma + j\Omega}{(2/T) - \Sigma - j\Omega} \tag{2.24}$$

From Eqn (2.23) it is evident that when $\Sigma < 0$ (left-half of s-plane), we obtain $|z| < 1$ which is the region inside the unit circle, and when $\Sigma > 0$ (right-half of s-plane), then $|z| > 1$ which is outside the unit circle. Thus the stability property is satisfied.

Following the above discussion, it is concluded that the bilinear transformation is superior to the two other transformations described in sections 2.5.1 and 2.5.2, also for the same reason, the bilinear transformation is employed to design SC resonators in the

next chapter.

There are two different versions of SC "BER" elements which may be employed to obtain bilinear SC filters from their active counterparts. These SC structures were first introduced by Rahim et al[64], and Temes[19], and are shown in Fig. 2.2(c) and (d) respectively. In Chapter 3 only BER elements of the type shown in Fig. 2.2 (d) are employed as the other version (Fig. 2.2 (c)) has one more capacitor and also has the problem of capacitor mismatch which affects the transfer function (frequency response) accuracy. Nevertheless, this latter BER element has been used in some SC circuits, for example, as an SC ladder load[77].

Finally, it should be mentioned that the design of bilinear transform SC filters is not restricted to replacing resistors in active RC filters by "BER" elements, but instead there exist several methods, including the transfer function approach, which result in bilinear SC filters with different circuit configurations[96].

CHAPTER 3: DESIGN OF PROGRAMMABLE SC RESONATORS FOR ADAPTIVE APPLICATIONS

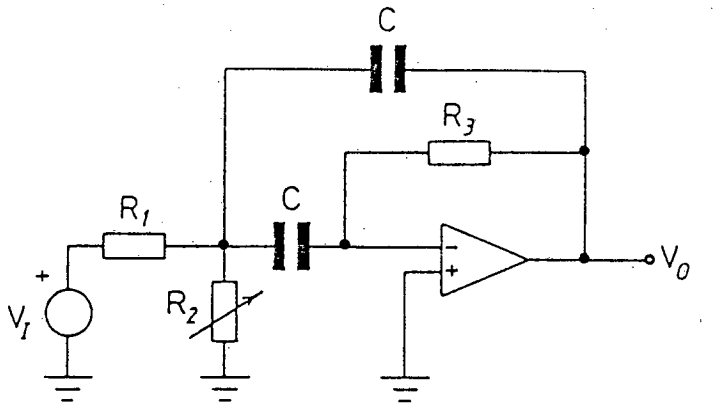
3.1 Introduction

The design of some selected single operational amplifier and multiple operational amplifier, programmable, switched capacitor, second order bandpass filters (biquad resonators) is investigated in the first part of the present Chapter. For the reasons explained in section 2.5.3, the bilinear z-transformation[144], and its associated resistor replacement[20] have been employed in deriving SC resonators from the active RC prototypes. During this investigation a general approach to the design of SC biquad filters with reduced sensitivity to the stray capacitances is proposed.

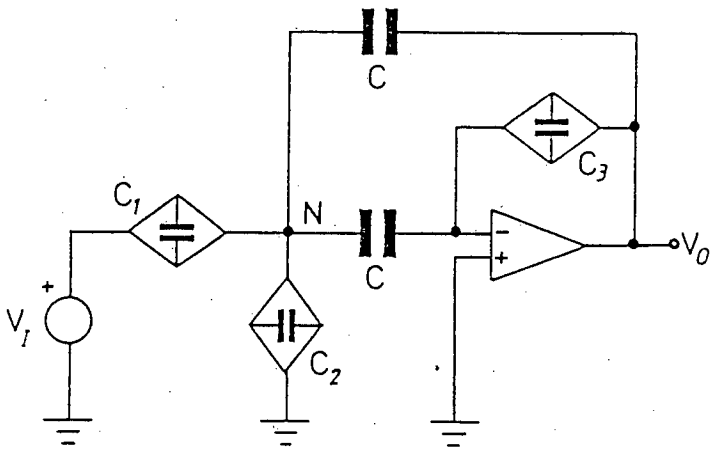
As a typical application to the above mentioned programmable SC resonators, they have been employed in a tracking filter topology[146]. The design method and experimental results for the SC tracking filter are presented in the second part of this Chapter. The successful design of SC tracking filters presented in this Chapter is regarded as one approach to the future realisation of fully-integrated MOS tracking filters.

3.2 Design of Single Operational Amplifier Biquad Resonators using SC "BER" Elements

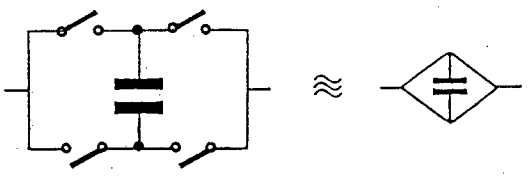
A single operational amplifier multiloop feedback (MLF) bandpass filter was selected as the analogue prototype for deriving its SC counterpart[214]. The motivation behind this selection was its low power consumption, the possibility of non-interactive tuning and, more importantly, its application in a type of tracking filter[147]. This prototype circuit is shown in Fig. 3.1(a).



(a)



(b)



(c)

FIG.3.1: Deriving a single-operational amplifier, switched-capacitor filter from an active-RC prototype using the switched-capacitor BER element.

(a) Circuit diagram of a single-operational amplifier active-RC biquad resonator.

(b) The switched-capacitor version of (a) using the switched-capacitor BER element.

(c) The simplified representation of the switched-capacitor BER element.

The transfer function of the prototype, continuous time active filter may be obtained by applying nodal analysis to the circuit shown in Fig. 3.1(a). Assuming that the operational amplifier has infinite gain and ideal characteristics[148]:

$$H(s) = \frac{Vo}{Vi} = \frac{-\frac{1}{R_1C}s}{s^2 + s.\frac{2}{R_3C} + \frac{1 + R_1/R_2}{R_1R_3C^2}} \qquad (3.1)$$

To find the gain at resonance G_o, centre frequency $\Omega_o = 2\pi f_o$, quality factor Q_a, and bandwidth $B_a = \frac{\Omega_o}{Q_a}$ of the analogue filter, Eqn (3.1) may be compared with the standard second-order equation for resonators[149]:

$$H(s) = \frac{G_oB_as}{s^2 + s.\frac{\Omega_o}{Q_a} + \Omega_o^2} = \frac{As}{s^2 + sB_a + \Omega_o^2} \qquad (3.2)$$

where $A = G_oB_a$,

which results in

$$\Omega_o = \frac{1}{C(R_3.R_{eq})^{\frac{1}{2}}} \qquad (3.3)$$

$$B_a = \frac{\Omega_o}{Q_a} = \frac{2}{R_3C} \qquad (3.4)$$

$$Q_a = \frac{R_3}{2(R_3.R_{eq})^{\frac{1}{2}}} \qquad (3.5)$$

and $$G_o = \frac{R_3}{2R_1} \qquad (3.6)$$

where $$R_{eq} = \frac{R_1R_2}{R_1+R_2}$$

From Eqns (3.3) to (3.6), it is evident that the centre frequency (Ω_o) of the filter could be varied by a single resistor R_2 without affecting B_a or G_o of the filter.

To derive the equivalent SC filter, we may first replace the resistors of the prototype active filter by SC "BER" elements. The resulting circuit is shown in Fig. 3.1(b). Then the equivalent z-domain SC transfer function could be obtained by replacing s in Eqn (3.1) by Eqn (2.18), and simultaneously replacing resistors (R_i's) by switched capacitors of value given by[20]:

$$C_N = \frac{1}{4 f_c R_N} \tag{3.7}$$

where f_c is the clock frequency. Following the above resistor substitution and after some algebraic manipulation using Eqn (3.2), the transfer fucntion of the SC filter is found to be:

$$H(z) = \frac{(A/K)(z^2 - 1)}{z^2 - \frac{2(1 - \Omega_o^2)}{K} \cdot z + \frac{1 - B_a + \Omega_o^2}{K}} \tag{3.8}$$

where $K = 1 + B_a + \Omega_o^2$ and A, B and Ω_o were defined in Eqn (3.2).

Since the bilinear z-transformation is a conformal mapping, Eqns (3.3) to (3.6) may be directly employed to find the centre frequency ω_o, bandwidth B, Q-factor and gain of the equivalent switched-capacitor filter. The only difference is the frequency warping effect which could be accounted for by prewarping method using Eqn (2.23). Thus, by substituting Eqn (3.7) in Eqns (3.3) to (3.6), for all resistors, we obtain:

$$\omega_o = \frac{4f_c \ (C_3 \ (C_1 + C_2))^{\frac{1}{2}}}{C} \tag{3.9}$$

$$B = \frac{8f_c C_3}{C} \tag{3.10}$$

$$Q = \tfrac{1}{2} \ (\frac{C_1 + C_2}{C_3})^{\frac{1}{2}} \tag{3.11}$$

$$G = \frac{C_1}{2C_3} \tag{3.12}$$

From the above equations it is observed that capacitor C_2 appears only in ω_o and Q definitions, but not in those for B or G. Therefore by changing capacitor C_2, the centre frequency of the SC resonator could be varied without affecting its gain or bandwidth.

In addition to capacitor C_2, clock frequency f_c could be used to tune ω_o of the SC resonator without affecting its Q or G. This property advantage is employed in designing an SC tracking filter which is described in section 3.4.

To demonstrate the concept, the SC filter shown in Fig. 3.1(b) was realised using discrete components. The nominal values selected for centre frequency, quality factor, and gain of the prototype filter were:

$$\omega_o = 1000 \text{ Hz}; \quad Q = 4; \quad \text{and}, \quad G = 1.$$

The routine sequence of design is as follows:

(a) The centre frequency ω_o of the SC filter is prewarped using Eqn (2.23), and a clock frequency of 8 kHz.

(b) The component values of the prototype active RC filter shown in Fig. 3.1(a) are obtained from standard design tables[149], for the new prewarped value of the centre frequency (Ω_o = 1055) and the nominal Q-factor and gain. These are:

R_1 = 603.54 kΩ; R_2 = 19.44 kΩ;
R_3 = 1207.07 kΩ and C = 1000 pF.

(c) Finally, the resistors of the active RC prototype are replaced by switched-capacitor values given by $(4f_cR)^{-1}$, with the "BER" structure. Capacitors in the RC active prototype remain unchanged. Capacitor values for the SC filter are obtained as:

C_{R1} = 52 pF; C_{R2} = 1608 pF and C_{R3} = 26 pF.

A low Q filter has been chosen because high Q would result in a high spread of capacitor values, and hence an increased chip area. The measured frequency response using 2.5% tolerance polystyrene capacitors, 4066 CMOS switches and an LF 356 operational amplifier, plotted with theoretical results (using SCNAP analysis programme; Appendix A) is shown in Fig. 3.2. The test board is shown in Fig.3.3.

Fig. 3.2 shows a large discrepancy (20%) between the measured and simulated results. This significant difference cannot simply be accounted for as the results of operational amplifier finite gain and bandwidth, or inaccurate capacitor values. This is because operational amplifiers with high gain (10^5) and wide bandwidth (5 MHz)

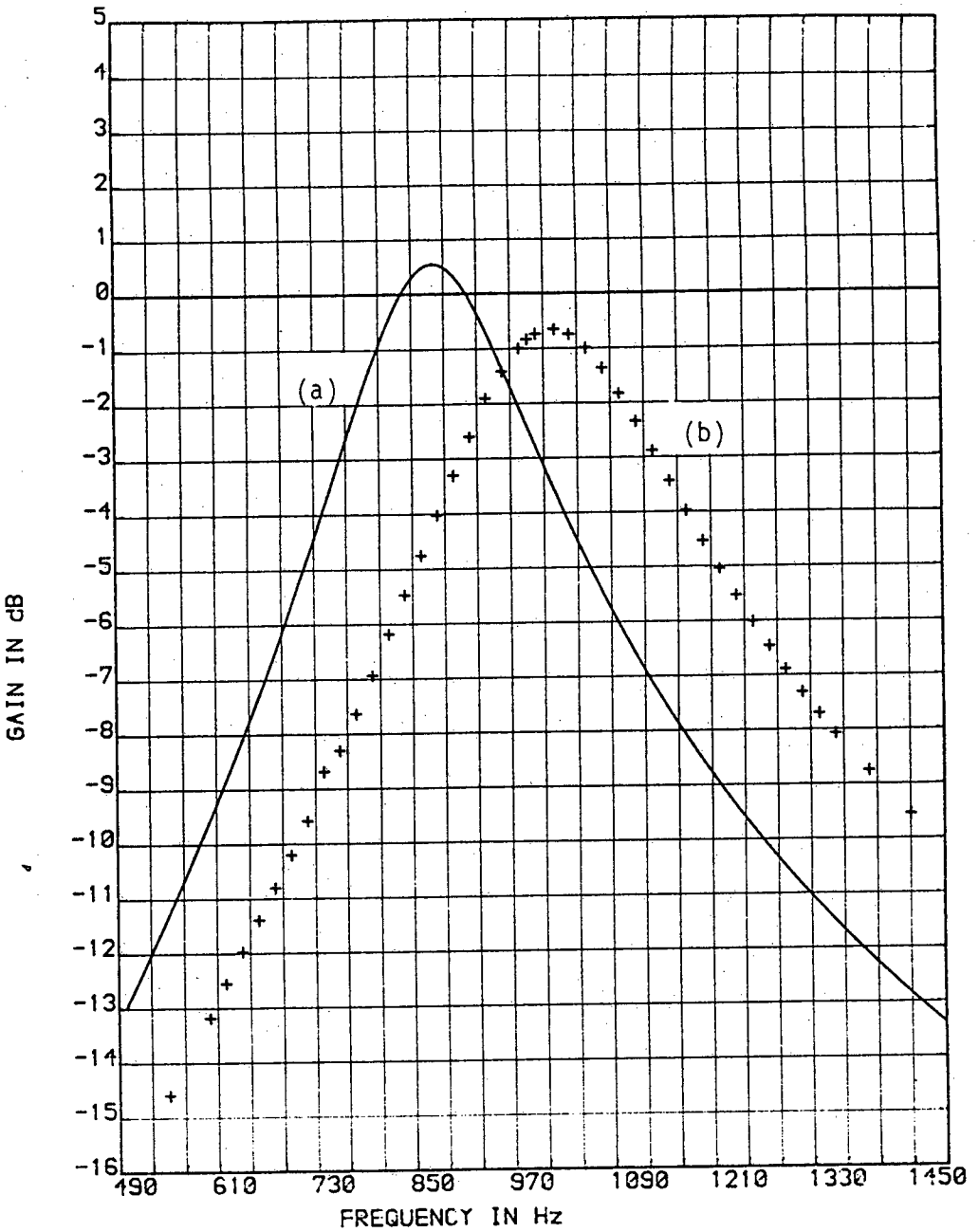


FIG.3.2: Simulated (a) and measured (b) frequency responses of the single-operational amplifier, switched-capacitor biquad resonator using the switched-capacitor BER element, shown in Fig.3.1(b). (C_2 = 1.33 nF.)

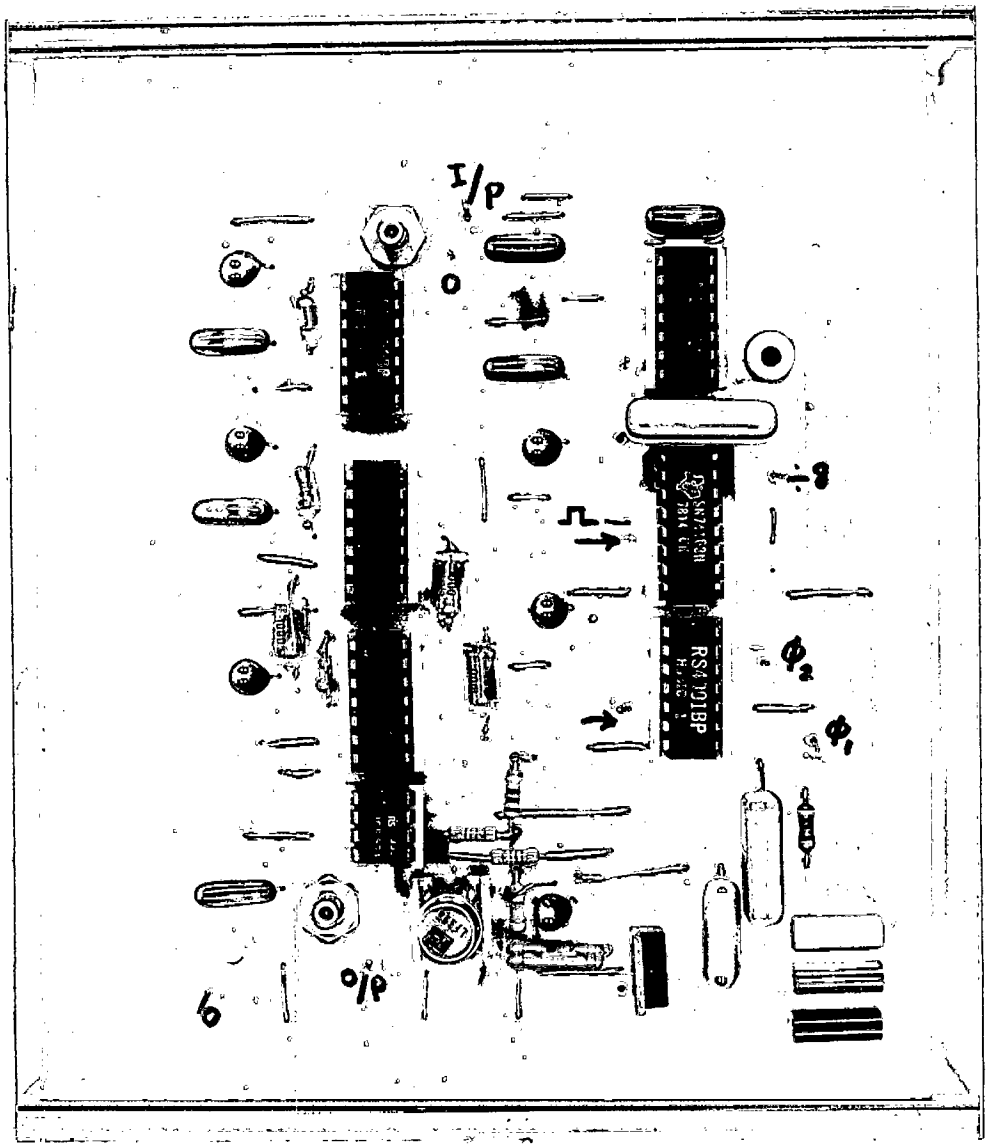


FIG.3.3: Photograph of the printed circuit board which contains the single-operational amplifier, switched-capacitor, biquad resonator described in section 3.2.

were employed, and the capacitor values were measured carefully before building the circuit.

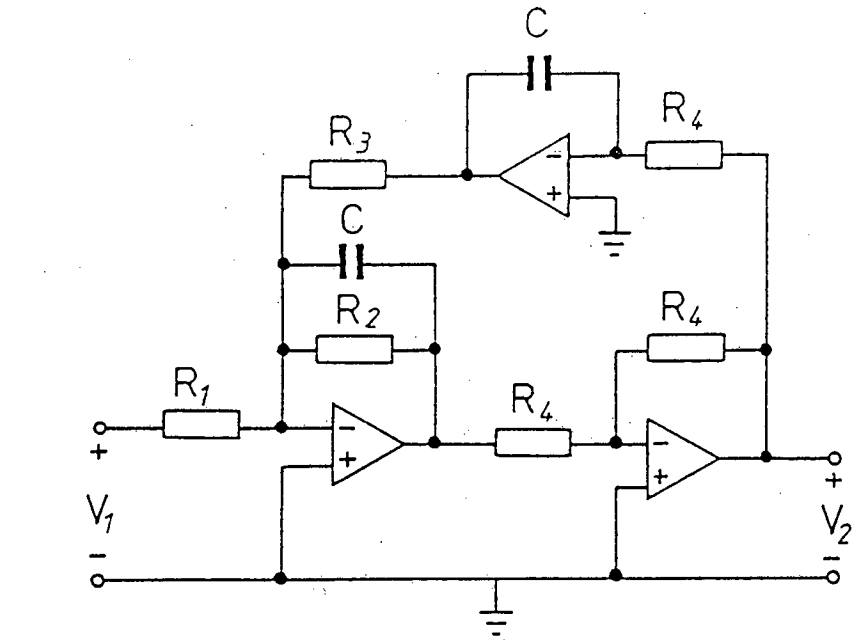
Computer simulation results, presented in Appendix B indicate that the floating node (N) in Fig. 3.1(b) and the parasitic capacitances associated with "BER" elements[150], are the major obstacles in achieving the accurate results.

For the reasons given above, and because the clock frequency (and not the individual capacitors) may well be employed to adjust the centre frequency of the SC resonator, the design of programmable SC resonators should not be restricted to the single operational amplifier biquad, described earlier. Any suitable circuit may be selected from the wide variety of biquad filters, as the active-RC prototype for the realisation of SC resonators.

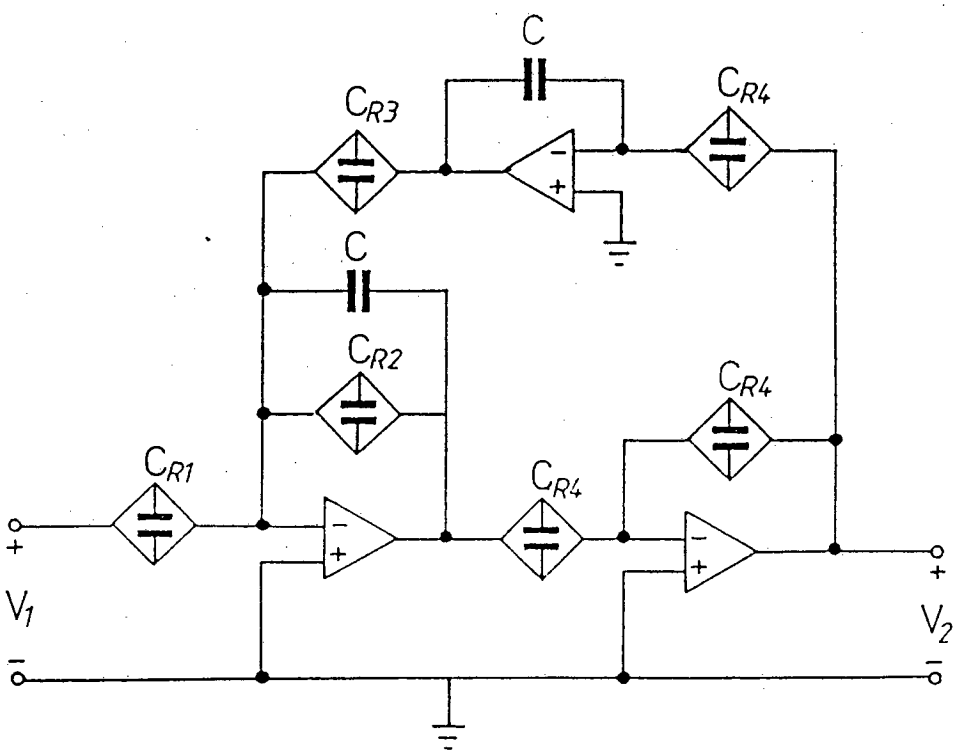
In the following section, the SC realisation of the well-known state-variable biquad filter[151] will be described. The conventional design described in section 3.2 will be improved for stray capacitance immunity, by introducing the modified "BER" elements.

3.3 Design of SC State-Variable Biquad Filter using Modified "BER" Elements

The prototype active-RC state-variable biquad, used in this section is of the type known as Tow-Thomas[151-156]. This biquad filter, which is shown in Fig. 3.4(a), unlike the single operational amplifier described in section 3.2, does not include any floating node; has an acceptable spread of capacitor values for medium and high Q realisation, and both bandpass and lowpass filtering functions



(a)



(b)

FIG.3.4: Deriving a state-variable switched-capacitor biquad filter, from an active-RC prototype using the switched-capacitor BER element.

(a) Tow-Thomas active-RC state-variable biquad filter.

(b) The switched-capacitor version of (a) using the switched-capacitor BER element.

are available simultaneously at different output terminals.

Design of the SC state-variable filter begins by replacing all resistors in Fig. 3.4(a) by "BER" elements as described in section 3.2. The resulting circuit is shown in Fig. 3.4(b). The "BER" elements are then replaced by "modified BER" elements. The modification of "BER" elements is demonstrated in Fig. 3.5 along with their equivalent (simplified) blocks. By applying the modified BER elements to the circuit of Fig. 3.4(b), a circuit results which has reduced sensitivity to the stray capacitances, because during either of the non-overlapping clock phases the switched-capacitors are grounded and hence any stray capacitance in the circuit discharges to ground. Another advantage of modified BER elements is that the whole inverter section in Fig. 3.4(b) can be replaced by a capacitor and four switches (compare Fig. 3.4(b) and Fig. 3.6).

This type of stray-insensitive circuit has already been used by several investigators[90,91,95,96], although without mentioning the original "BER" element. As it is shown in Fig. 3.5, the modification of SC BER elements results in structures that are either equivalent to SER elements (Fig. 3.5(b)), or are equivalent to PER elements (Fig. 3.5(c)). Therefore, after substituting the modified BER elements for resistors in the active-RC biquad, the transfer function of the resulting SC filter is not simply obtained by replacing s with $2(z-1)/[T(z+1)]$ (Eqn (2.18)), rather the modified SC filter should be analysed by first writing the charge equations of the circuit at different nodes and then taking the z-transform of the resulting difference equation to find the desired transfer function.

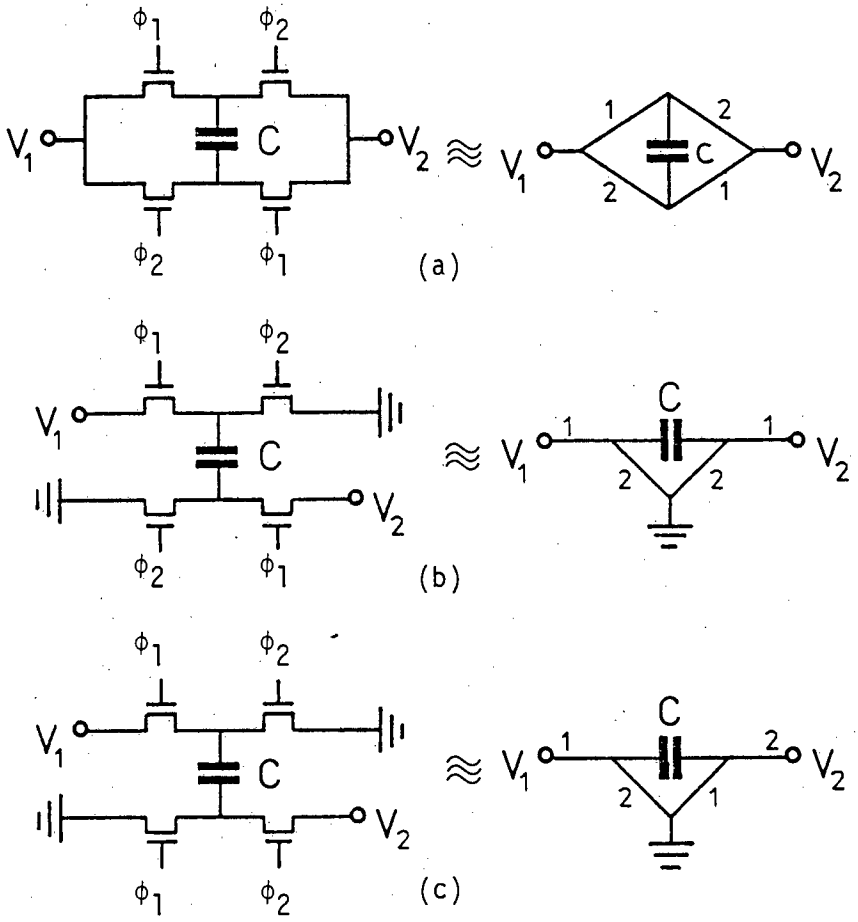


FIG.3.5: Modifications of the switched-capacitor BER element for stray-insensitive circuit realisations.

(a) The original switched-capacitor BER element and its simplified representation.

(b) Non-inverting "modified BER" element and its simplified representation.

(c) Inverting "modified BER" element and its simplified representation.

The SC state-variable biquad using the modified BER elements is shown in Fig. 3.6. Numbers 1 and 2 in this figure indicate the clock phases during which switches are closed, and is a convention adopted throughout this thesis. Two filtering functions, i.e. bandpass and lowpass functions, are available simultaneously from nodes V_1 and V_2 respectively, but the bandpass filter output (at node V_1) is of present interest.

As mentioned earlier, to obtain the transfer function and the expressions for ω_o and Q, which determine the pole positions of the filter, charge equation of the circuit at different nodes should be written. Referring to Fig. 3.6 for the first operational amplifier, the following equation could be obtained:

$$V_1C_1(nT) = V_1C_1(n-1) + V_{IN}a_1C_1(n-1)T - V_1a_2(nT) + a_4C_1V_2(n-1)T \tag{3.13}$$

and for the second operational amplifier:

$$V_2C_2(nT) = V_2C_2(n-1) - V_1a_3C_2(nT) \tag{3.14}$$

where a_i are the capacitor ratios and $V_ia_jC_k(nT)$ are the charge stored in capacitor a_jC_k at time nT.

By taking the z-transform from both sides of Eqns (3.13) and (3.14) and after some algebraic manipulation the transfer function of the SC resonator at node V_1 is obtained as:

$$H(z) = \frac{V_1(z)}{V_{IN}(z)} = \frac{a_1\,(z-1)/(1+a_2)}{z^2 - z\left(\frac{2 + a_2 - a_3a_4}{1 + a_2}\right) + \frac{1}{1 + a_2}} \tag{3.15}$$

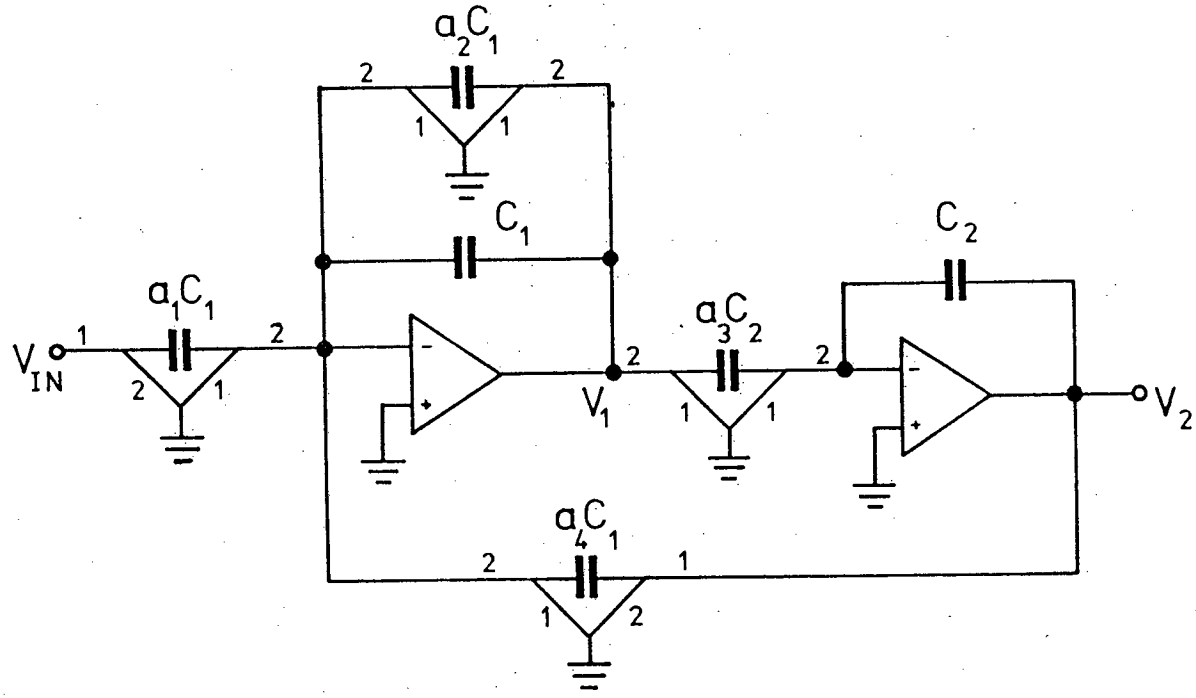


FIG.3.6: A stray-insensitive circuit for the state-variable, switched-capacitor biquad resonator shown in Fig.3.4(b), using the modified BER elements.

This is the exact transfer function of the circuit for V_1 output. To obtain the capacitor ratios and hence the capacitor values of the above SC biquad filter shown in Fig. 3.6, it is necessary to obtain the desired expressions for ω_o and Q of the filter. This is performed by comparing Eqn (3.15) with a bilinear z-transform transfer function of the form given in Eqn (3.8). Following the above procedure, and after a lengthy but straightforward algebraic calculation, the following relations for ω_o and Q are obtained:

$$\omega_o = 2 \left(\frac{a_3 a_4}{4 + 2a_2 - a_3 a_4}\right)^{\frac{1}{2}} \tag{3.16}$$

and

$$Q = \left(\frac{a_3 a_4 (4 + 2a_2 - a_3 a_4)}{2a_2}\right)^{\frac{1}{2}} \tag{3.17}$$

in which the clock period T has been normalised to unity.

Assuming equal values for a_3 and a_4 and for a resonator with Q = 15 and ω_o = 1000 x 2π rad/sec and clock frequency of 8 kHz, the following capacitor ratios are obtained:

$$a_2 = 0.0356689$$

$$a_3 = a_4 = 0.7708147$$

and $$a_1 = 0.032.$$

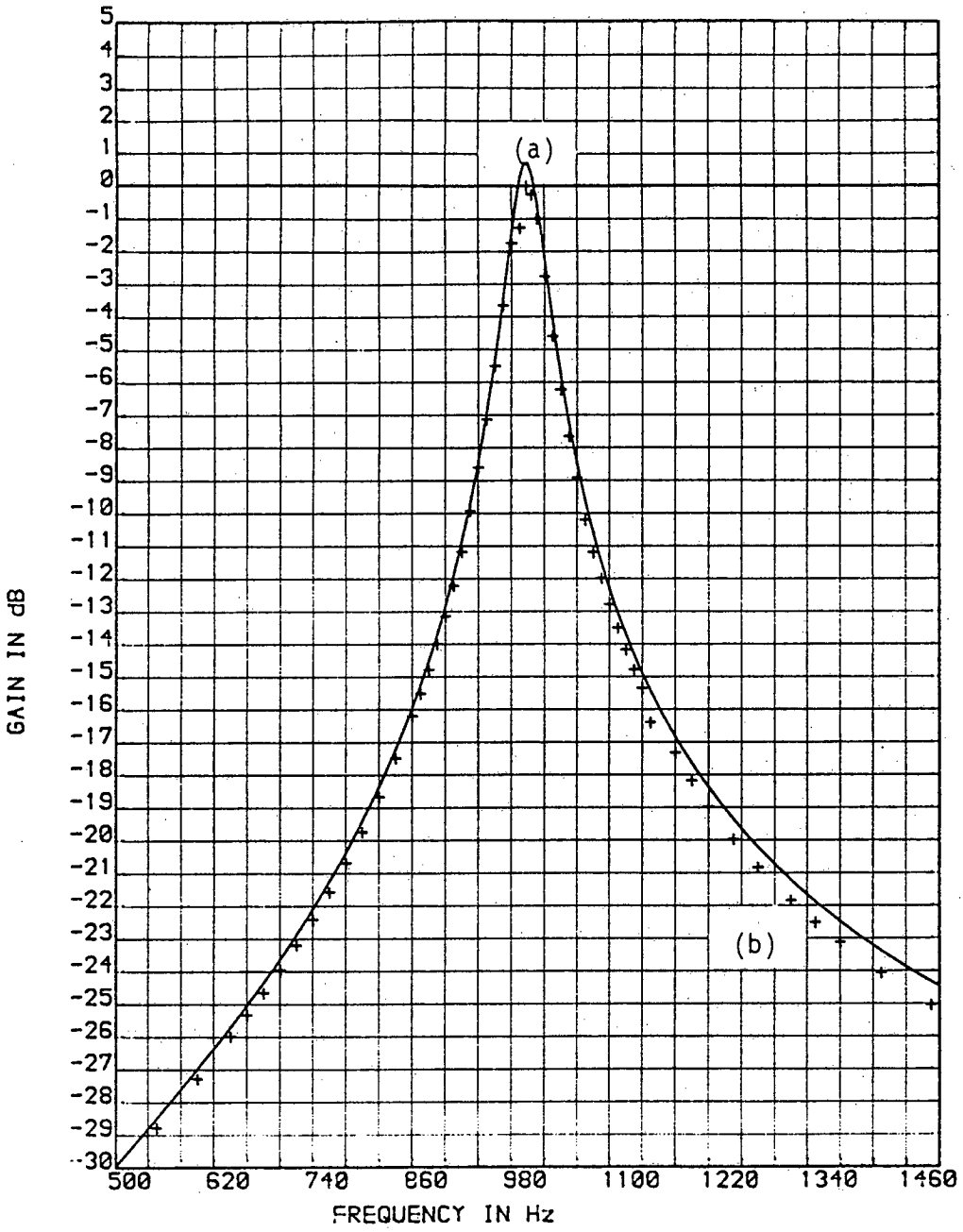


FIG.3.7: Simulated (a) and measured (b) frequency responses of the stray-insensitive, state-variable, switched-capacitor biquad resonator, shown in Fig.3.6.

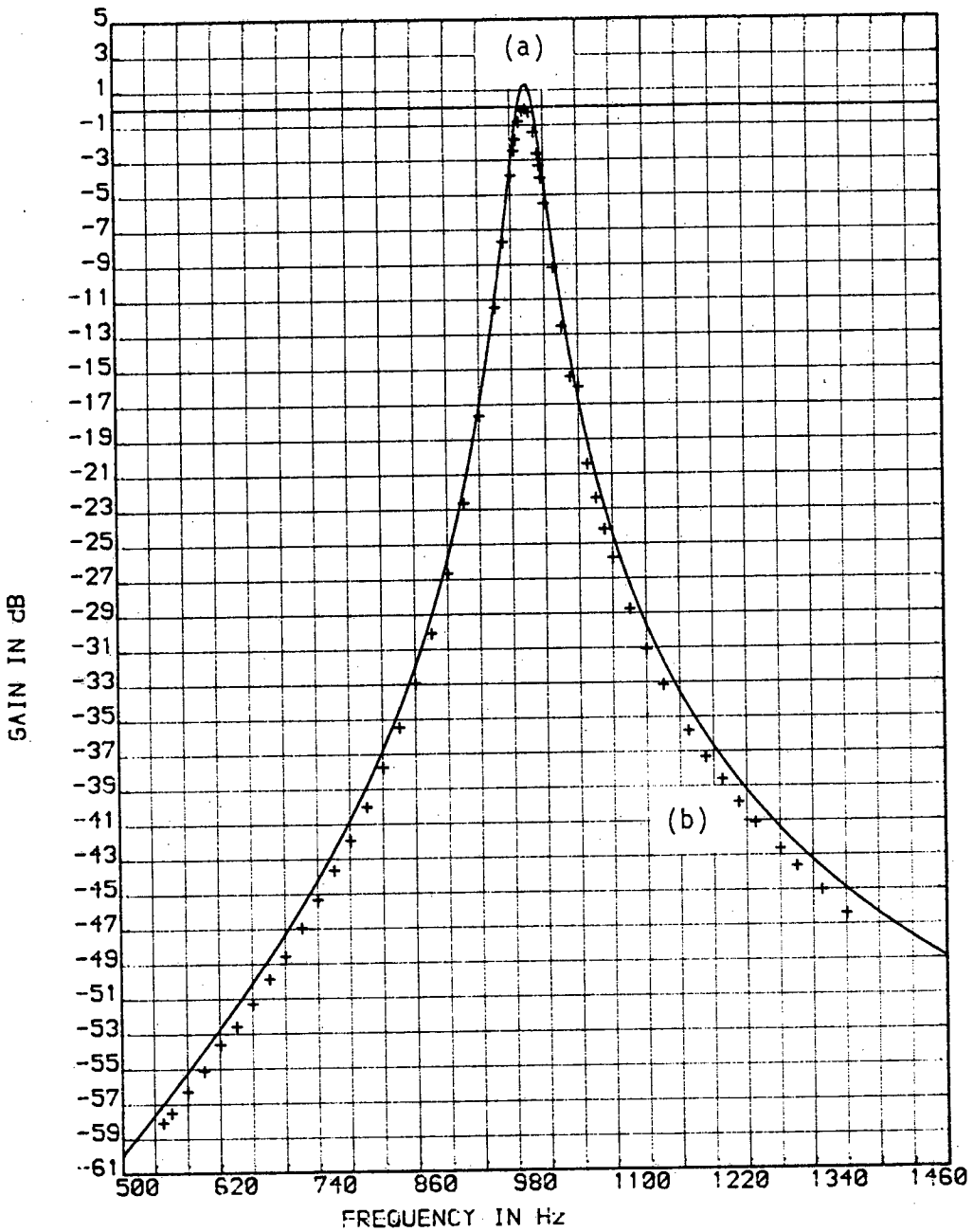


FIG.3.8: Simulated (a) and measured (b) frequency responses of a fourth-order, stray insensitive, switched-capacitor resonator, formed by two cascaded second-order sections shown in Fig.3.6.

The SC circuit shown in Fig. 3.6, was built with discrete components and the above capacitor ratios. The measured and calculated frequency responses are compared in Fig. 3.7, in which the measured and calculated frequency responses are much closer compared to the previous direct design described in section 3.2. This good agreement is due to the stray insensitive structure of the biquad in Fig. 3.6, and the exact analysis leading to the exact design of the circuit.

An attempt was made to realise a higher order resonator by cascading the above second-order biquad section. The result is a fourth-order resonator for which the measured and calculated frequency responses are compared in Fig.3.8. The close agreement between the measured and simulated results indicates the reliability of the design method described in this section.

A picture of all the SC filters realised in this section is shown in Fig. 3.9. This test board also includes the SC tracking filter, which will be described in the next section.

3.4 Tracking Filter Implementation using Switched-Capacitor Bandpass Filters

Tracking filters are a class of "synchronous control systems"[157], in which a form of phase, frequency or amplitude coherence between the input and output signals is provided by automatic means[158]. In general, a tracking filter is employed to detect a modulated signal, or to recover a weak signal deeply contaminated with noise.

When the input signal to a system varies widely in frequency

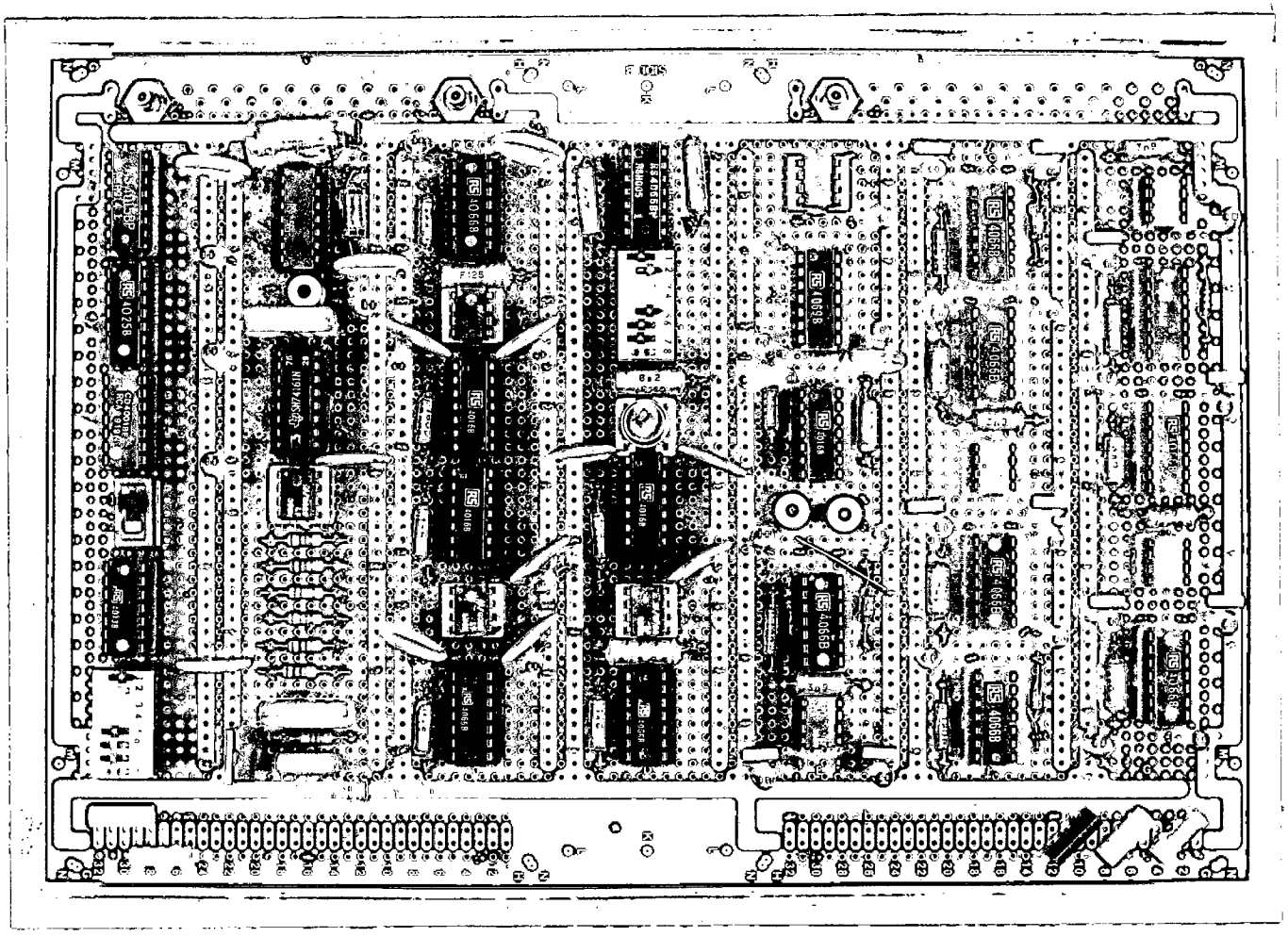


FIG.3.9: Photograph of the stripboard which contains the switched-capacitor biquad resonators, described in sections 3.3 and 3.4, and the switched-capacitor tracking filter described in section 3.4.3.

(and phase) the presence of a conventional wideband filter would not sufficiently reject the input noise and so it does not provide a good output signal-to-noise ratio. Noise can be rejected by a narrow band filter, but if the filter is fixed the signal will almost never be within the passband. For a narrow-band filter to be usable it must be capable of tracking the signal. The main purpose of this section is to demonstrate how the centre frequency of the SC bandpass filters designed in section 3.3 could be controlled automatically in order to track the input signal. Since the important parameters of the tracking system, e.g. tracking range and noise rejection, are determined by the PLL, a part of the present section is devoted to its fundamental concepts. A tutorial paper by Gupta[159] describes different types of PLLs and presents a comprehensive and useful bibliography of the subject.

3.4.1 The Basic PLL

The PLL is basically a servo system comprised of a phase sensitive detector (or phase comparator) PD, a lowpass filter LP, an error amplifier A, a voltage-controlled oscillator VCO. Fig. 3.10 shows the block diagram of a PLL including the above mentioned components as well as a divide by N counter for frequency multiplication applications. The VCO is an oscillator whose frequency is controlled by an external voltage. When an input signal is applied to the system the phase comparator compares the phase and frequency of the incoming signal with the VCO frequency and generates an error voltage proportional to the phase difference between the two signals. When a divide by N counter is present in the loop, the phase comparator generates an error voltage proportional to the phase difference between the incoming signal

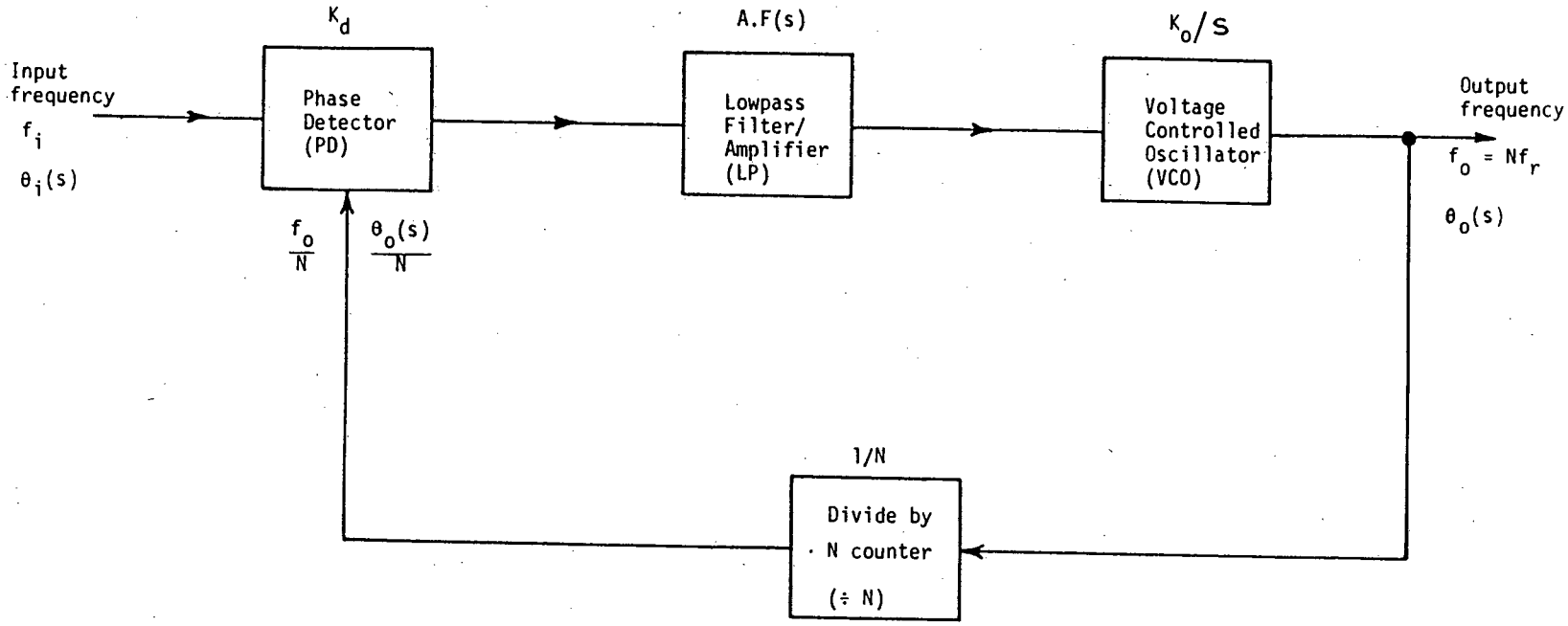


FIG.3.10: Block diagram of the phase-locked loop including the divide by N counter.

and the output signal of the divide by N counter. This voltage is then filtered, amplified and applied to the control input of the VCO. The control voltage forces the VCO frequency to vary in a direction that reduces the frequency difference between the two signals. When the loop is "locked", the control voltage is such that the frequency of the VCO is exactly equal to (or N times, if divide by N counter is present) the average frequency of the input signal. The range of frequencies over which the loop can maintain lock is called the "lock range" or the "tracking range". The "capture range" is the band of frequencies over which the loop can acquire lock from an unlocked condition[158].

In the following section, the type of PLL employed in our tracking filter will be analysed to gain more insight into the system.

3.4.2 Analysis of PLL Including Divide by N Counter

PLLs have both linear and non-linear elements, but are normally analysed using the Laplace transform method. This is justified if the VCO operates in the linear region of its transfer curve, and if the phase difference between the input and VCO output signals is sufficiently small[146]. These conditions are satisfied during the lock region. Under the above conditions, the PLL can be treated as a linear feedback system, and its transfer function may be obtained using established methods[158-162]. Using the terminology given in Fig. 3.10, and applying negative feedback, closed loop gain expression, we obtain:

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d \cdot \frac{K_o}{s} \cdot A \cdot F(s)}{1 + K_d \cdot \frac{K_o}{s} \cdot A \cdot F(s) \frac{1}{N}}$$

$$= \frac{K_d K_o A \, F(s)}{s + K_d K_o A \, F(s) \cdot \frac{1}{N}} \qquad (3.18)$$

where θ_o is the output phase of the VCO; θ_i is the input or reference phase; K_d is the phase detector gain factor in volts per radian; K_o is the conversion (or gain) factor between VCO frequency and the control voltage, in radians per second per volt; A is the gain of the amplifier used in the loop; F(s) is the voltage transfer function of the lowpass filter; and N is the counter's division factor. The product of dc gains of all the loop elements is called loop gain, K_v, i.e.

$$K_v = K_d \, K_o \, A \qquad (3.19)$$

which has the dimension of $(\text{sec})^{-1}$.

To obtain the final closed loop transfer function, it is useful to substitute for the lowpass filter transfer function F(s). In the case of a simple RC filter, which was used in our experiment

$$F(s) = \frac{1}{1 + s\tau} \qquad (3.20)$$

where $\tau = RC$ is the time constant of the lowpass filter. Substituting the above value of F(s), in Eqn (3.18), results in the following

closed loop transfer function of the PLL:

$$H(s) = \frac{K_v/\tau}{s^2 + (1/\tau)\, s + K_v/N\tau} \tag{3.21}$$

which is a second order transfer function with positive gain. From Eqn (3.21) it is possible to obtain the loop natural frequency ω_n and damping factor ζ. The values of ω_n and ζ are particularly important in terms of overall stability and transient response. These are obtained by comparing the denominator of Eqn (3.21) with the following equation[163]:

$$D(s) = s^2 + 2\,\zeta\omega_n\, s + \omega_n^2. \tag{3.22}$$

Following the above procedure we obtain

$$\omega_n = (K_v/N\tau)^{\frac{1}{2}} \tag{3.23}$$

and

$$\zeta = \tfrac{1}{2}.(N/K_v\tau)^{\frac{1}{2}}. \tag{3.24}$$

Since the constants K_d, K_o and N are usually fixed due to other design constraints, τ is used as variable to set ω_n and ζ. This indicates the significance of the lowpass filter in defining the loop noise bandwidth (ω_n) and its transient response (ζ).

Frequency response of type NE 565 PLL[164] is shown in Fig. 3.11. This response is based on Eqn (3.21) using the values K_v = 11883(sec)$^{-1}$, τ = 2 msec and N = 8. From Fig. 3.11, the values of ω_n and ζ are obtained as: 860 rad/sec. and 0.3 respectively.

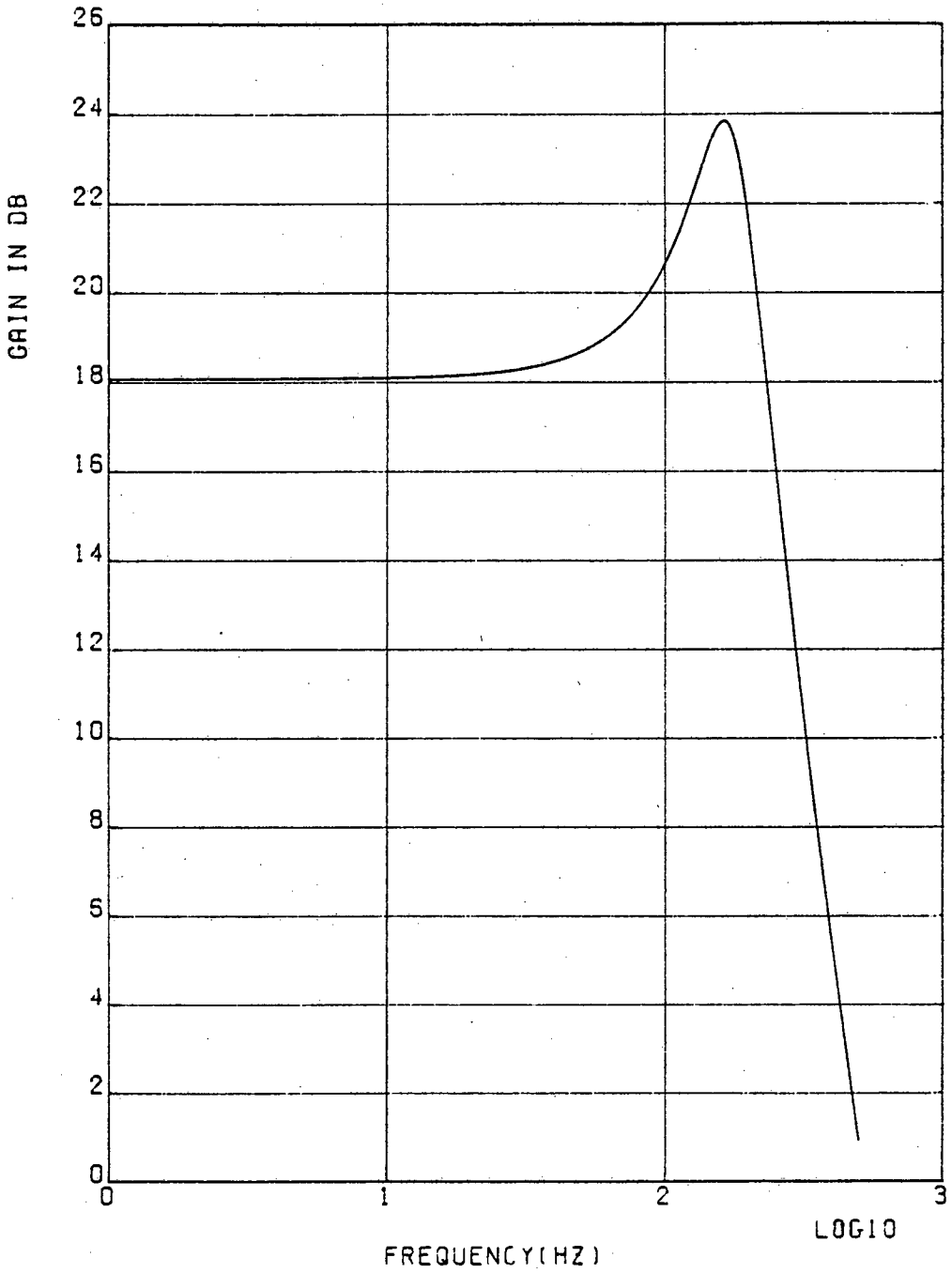


FIG.3.11: Frequency response of the experimental phase-locked loop including the divide by N counter.

3.4.3 Description of SC Tracking Filter

The block diagram of the SC tracking filter, using the phase-locked loop principle described in section 3.4.1, is shown in Fig. 3.12. As shown in this figure, the above tracking filter comprises an NE 565 PLL, a second order SC bandpass filter described in section 3.3, a pulse shaping circuit to provide the necessary two-phase non-overlapping clocks for the SC bandpass filter, and a digital counter. This digital counter is placed between VCO and PD of the PLL to provide the required multiplication factor (N) of the PLL, and to obtain the desired clock-to-centre frequency ratio for the SC bandpass filter. The main reasons for employing type NE 565 PLL were its economy, and flexibility in the sense that the loop could be broken between the VCO and phase comparator (PD) to allow the insertion of a counter.

Using the above combination, the fundamental frequency of the divided VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication (N) is determined by the counter. Now if the SC filter is designed to have a clock-to-centre frequency ratio equal to N, then the centre frequency of the SC filter will be locked to the input frequency.

3.4.4 Measurement of Tracking and Capture Ranges

The tracking and capture ranges were defined in section 3.4.1. Using the empirical relations given for NE 565 PLL[164], the value of the tracking (lock) range is obtained as:

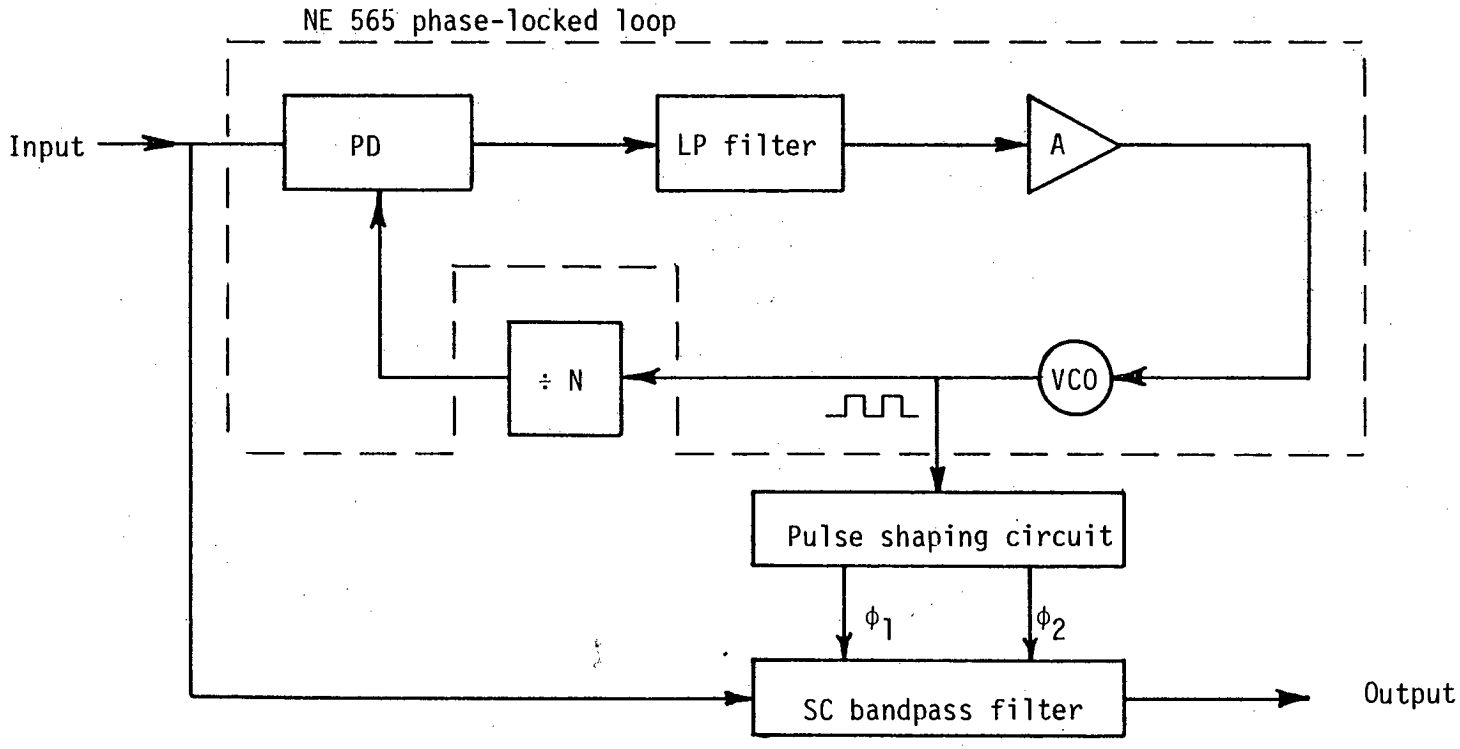


FIG.3.12: Block diagram of the experimental switched-capacitor tracking filter.

$$f_L \simeq \pm \frac{f_{VCO}}{V_{CC}} = \pm \frac{8000}{15} = \pm 533 \text{ Hz} \qquad (3.25)$$

where f_{VCO} is the VCO frequency during lock, and V_{CC} is the total power supply voltage.

Also the capture range is given by[164]:

$$f_{ca} \simeq \pm \frac{1}{2\pi} \left(\frac{2\pi f_L}{\tau}\right)^{\frac{1}{2}} = \pm 206 \text{ Hz} \qquad (3.26)$$

where $\tau = RC \simeq 2 \times 10^{-3}$ sec, is the time constant of the RC filter employed in the PLL.

The frequency response of the SC tracking filter using the spectrum analyser is shown in Fig. 3.13, from which the tracking and capture ranges can be measured. The measured values of the tracking and capture ranges are ± 620 Hz and ± 200 Hz respectively, which are close to the values obtained from the empirical relations in Eqns (3.25) and (3.26). Note that the centre frequency of the SC resonator was designed to be at 1000 Hz, and since N = 8, the VCO (clock) was running at $f_c = 8f_{VCO} = 8000$ Hz.

It has been demonstrated[165] that using active-RC filters improves the tracking and capture ranges of the PLL and hence the tracking filter. Unfortunately, in the NE 565 type PLL, use of active filters was not allowed, which is considered as a disadvantage. However, for the purposes of this chapter, which were to design and investigate a simple and practical SC tracking filter, the above mentioned PLL was quite adequate.

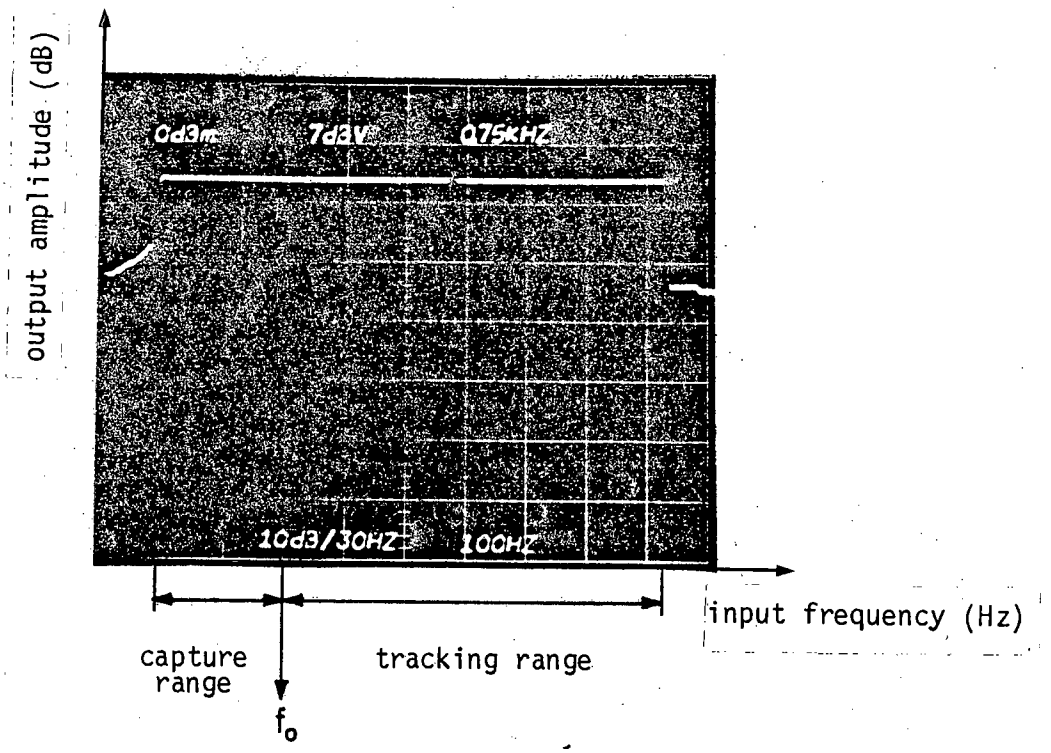


FIG.3.13: Spectrum analyser picture of the frequency response of the experimental switched-capacitor tracking filter.

3.4.5 Noise Rejection

To observe the noise rejection of the SC tracking filter, a noisy input was applied to the input of the tracking filter. The output signal of the tracking filter, as well as its noisy input, are shown in Fig. 3.14, to show the noise rejection.

To improve the noise rejection, the passband of the lowpass filter (inside the PLL) or the SC bandpass filter, may be reduced. But according to Eqns (3.23), (3.24) and (3.26), change of the lowpass filter passband would affect the transient response and capture range of the tracking system. Therefore the SC bandpass filter may be used to improve the noise rejection of the tracking filter. This is one advantage of using a bandpass filter in conjunction with the PLL. The other advantage is that using a narrow-band filter preserves the phase and amplitude of the incoming signal, while the PLL alone would suppress them[157].

Since all the elements in the SC tracking filter presented in this Chapter, including the PLL[166], are realisable in MOS technology, it is concluded that the implementation of a single chip MOS tracking filter is feasible.

(a)

(b)

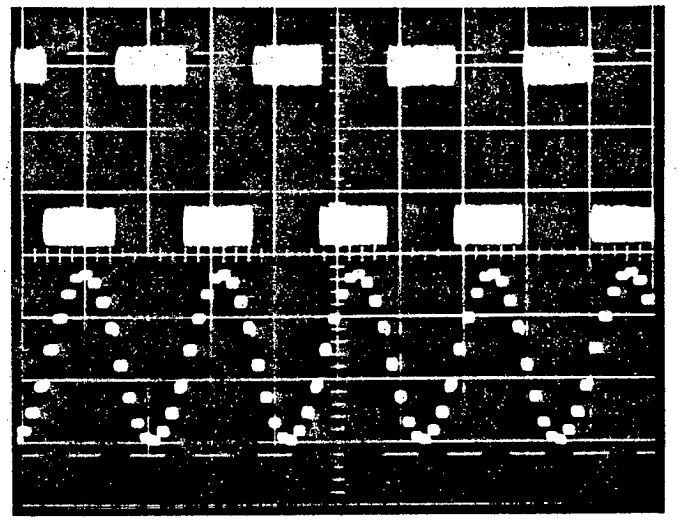


FIG.3.14: Noise rejection capability of the experimental switched-capacitor tracking filter.

(a) Input signal added with noise.

(b) Output signal from the experimental switched-capacitor tracking filter.

Vertical scale: 1 V/div.

Horizontal scale: 0.5 msec./div.

CHAPTER 4: EXACT DESIGN OF SWITCHED-CAPACITOR ALL-POLE LOWPASS LADDER FILTERS

4.1 Introduction

Active biquad filters for which some switched-capacitor counterparts were derived and examined in Chapter 3, are useful and adequate for many simple and non-precision filtering applications. However, in many communication applications, the need is for high order ($n > 2$), high precision frequency selective filters. Although it is possible to construct high order filters by cascading first and second order sections because of the inherent sensitivity of active biquad filters to their passive and active components, the high order filters made by cascading low order sections will have even higher sensitivity. Consequently, high order precision filters are not usually designed using the cascade approach.

It is now generally accepted[17] that SC filters have the same order of sensitivity as their active-RC prototypes from which they are derived. Therefore, prototypes with better sensitivity properties are invariably preferred. A well-known, minimum sensitivity filter structure is the doubly terminated lossless RLC ladder filter (c.f. Fig. 4.2(a)), which has zero first order sensitivity to component changes in the frequencies where the filter power gain is maximum[12,151]. In section 4.2, sensitivity of the doubly terminated RLC filter will be described in more detail. In general, high order active filters derived from the direct approach (as opposed to the cascade approach) using doubly terminated RLC filters have about 10 times better sensitivity compared to singly terminated RLC filters and about 20 times better sensitivity compared to the cascade approach using low order

active-RC sections[167]. Conventional SC ladder filters, which were first introduced by Allstot et al[13], are the sampled-data version of active leapfrog filters proposed by Girling et al[168]; these in turn are the active simulation of passive RLC ladder filters. Therefore SC ladder filters benefit from the minimum sensitivity of passive RLC ladder filters; a point to be described in section 4.3.

Although the introduction of SC ladder filters provided a suitable method for implementing high order, fully integrated frequency selective filters, it was soon found that early design methods were not optimum. This meant that to obtain a high precision filter some assumption had to be adopted which at the same time limited the performance of the filter. For example, if the ratio of the passband edge of the designed SC ladder filter to the sampling frequency is not low enough (say less than 5%) then the resulting SC filter will not resemble the original RLC ladder filter, i.e. its frequency response will be affected. To overcome this problem to some extent, the passband edge to clock frequency must be very low, typically less than 3%, but this remedy will obviously limit the useful frequency range of the SC filter and results in high capacitor ratios[7]. This point will become clearer in section 4.6, where an example of conventional (approximate) design is given.

Among the different design approaches suggested to overcome the above mentioned problems[66,74-79], the concise design method proposed by Scanlan[17] is adopted by the author of this thesis to design an SC lowpass ladder filter in NMOS integrated circuit form, to validate its applicability at high percentage (> 10%) passband edge to clock frequencies. The design and experimental results for integrated SC

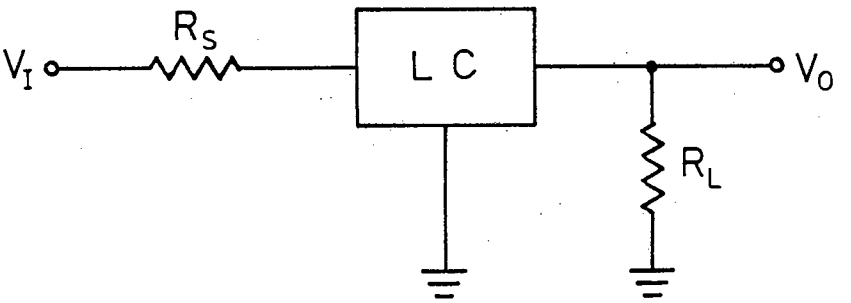
third-order, maximally flat, all-pole lowpass ladder filters is given in Chapter 6.

In the next sections, discussion of the low sensitivity of the doubly terminated RLC ladder filter, also derivation of SC all-pole lowpass ladder filters from passive LC prototypes, and the exact design of SC lowpass ladder filters will be described. Since the realised filter in integrated circuit form was chosen for illustration to be a third-order, maximally flat, all-pole lowpass filter, all derivations and worked examples hereafter are modified accordingly.

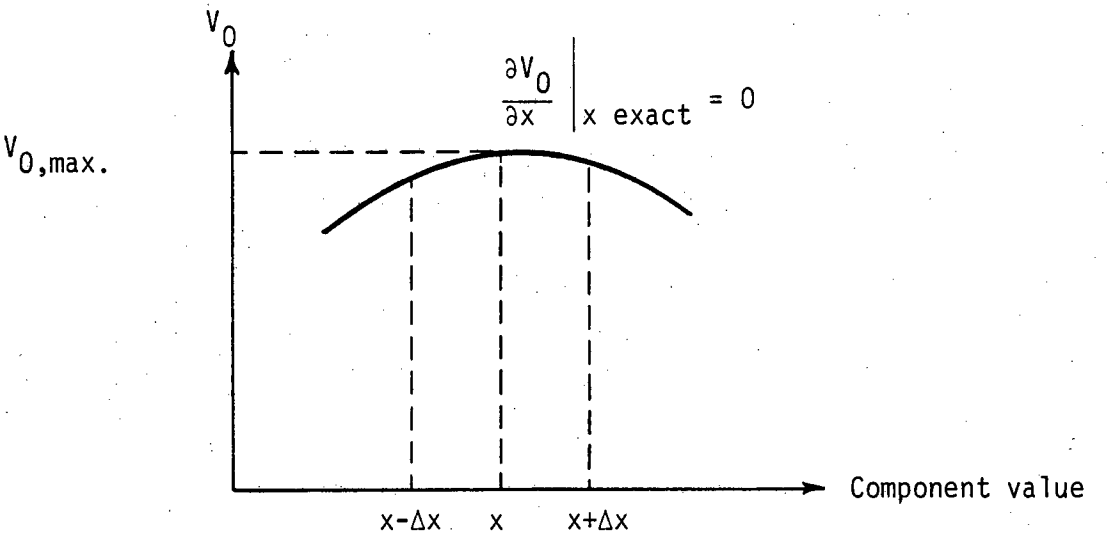
4.2 Low Sensitivity of Doubly Terminated RLC Ladder Filters

There are several methods to prove the low sensitivity of doubly terminated lossless ladder filters[1,12,22,23], but the heuristic argument due to Orchard[12,151] is employed in this section because of its simplitiy and because it avoids lengthy mathematical derivations.

Doubly terminated lossless networks, typified in Fig. 4.1(a), can always be designed to have maximum power transfer from source to load, under certain conditions. For example, where the source resistance, R_s, is equal to the load resistance R_L, and where the reactive elements are equal to their ideal values. This suggests that under some specific conditions, the output power V_0^2/R_L will be maximum and hence the output voltage V_0 is maximum. In this case any change in the reactive element values X, either up or down, can only cause the power transferred to the load to decrease (or V_0 to decrease). Thus the quadratic curve shown in Fig. 4.1(b), is obtained which shows



(a)



(b)

FIG.4.1: Minimum sensitivity of the doubly-terminated LC ladder filter:

(a) A doubly-terminated LC filter.

(b) First-order sensitivity curve for a doubly-terminated LC ladder filter.

the relation between the output voltage and the change in reactive element values. At maximum V_0, the following relationship always exists:

$$\left.\frac{\partial V_0}{\partial X}\right|_{X \text{ exact}} = 0 \qquad (4.1)$$

Since the sensitivity is directly related to Eqn (4.1), it is concluded that the first order sensitivity of the doubly terminated lossless networks is zero at frequencies where the output power is maximum. In fact, in the region close to the exact value of any reactive element, the sensitivity of the above network is approximately zero, because the gain (or loss) is a smooth continuous function. Therefore such a passive realisation should have a low sensitivity in the entire passband. Note that the above argument is not valid for the sensitivity in the transition and stopband regions[151], but this is not a significant problem in most of the filter applications.

The above unique property has made doubly terminated networks very attractive, so that these networks are mostly selected as prototypes for deriving inductorless active RC filters, SC ladder and many other filters.

4.3 Active Simulation of Passive, All-Pole, Lowpass Ladder Filters

As mentioned in sections 4.1 and 4.2, design of high order and high precision filters, with stringent requirements such as telephone channel filters, should preferably be based on the doubly terminated LC ladder filters because of their extremely low sensitivity to element variations, and also because of their well established theory

and design.

A simple reciprocal type of resistively terminated LC ladder network is shown in Fig. 4.2(a) for the third-order, all-pole, lowpass case. Choice of this simple network does not affect the generality of the approach as the realisation of the higher order filters is possible by repeating the blocks corresponding to series inductors and shunt capacitors. The network shown in Fig. 4.2(a) is called a T-type ladder, in contrast to a π-type ladder in which the first and last reactive elements in the circuit are shunt capacitors. The π-type ladder is useful when the inductor simulation approach is employed in designing active-RC or switched-capacitor filters, because it contains less inductors.

For the development of the subject it is useful to obtain the voltage-current relations for the series and shunt branches according to Kirchoff's laws. In so doing for Fig. 4.2(a), we obtain the following relationships:

$$I_1 = \frac{1}{L_1 s + R_S} (V_{IN} - V_1) \tag{4.2}$$

$$V_1 = \frac{1}{C_2 s} (I_1 - I_L) \tag{4.3}$$

$$I_L = \frac{1}{L_3 s + R_L} V_1 \tag{4.4}$$

where $s = j\Omega$.

The desired transfer function of the above ladder (or any odd degree) network is:

$$H_{21} = \frac{I_L}{V_{IN}} \tag{4.5}$$

For the reasons mentioned earlier, including the existence of bulky inductors at low frequencies, attempts have been made to simulate the behaviour of the passive LC ladder networks, by an active circuit containing only resistors, capacitors and operational amplifier. In fact, any circuit which could realise the Eqns (4.2) to (4.4) will provide the same transfer function as Eqn (4.5). One of the possible circuits is shown in Fig. 4.2(b), for which the following equations exist:

$$V_1' = T_1 (V_{IN} - V_1) \tag{4.6}$$

$$V_1 = T_2 (V_1' - V_L') \tag{4.7}$$

$$V_L' = T_3 V_1 \tag{4.8}$$

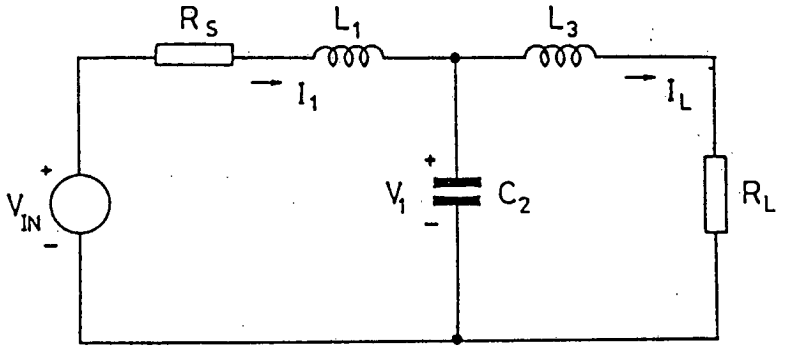
Now comparing Eqns (4.6) to (4.8) with Eqns (4.2) to (4.4) one may conclude that, if the blocks T_1, T_2 and T_3 are defined by the following equation, i.e.:

$$T_1 = k \frac{1}{L_1 s + R_S} \tag{4.9}$$

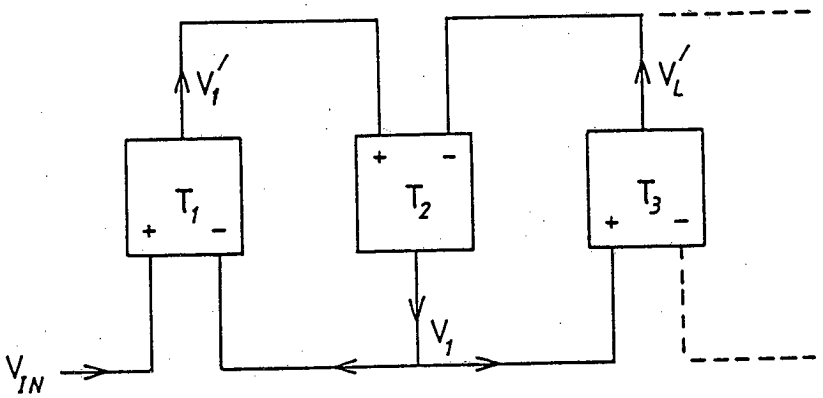
$$T_2 = k^{-1} \frac{1}{C_2 s} \tag{4.10}$$

$$T_3 = k \frac{1}{L_3 s + R_L} \tag{4.11}$$

(k being a scaling factor),



(a)

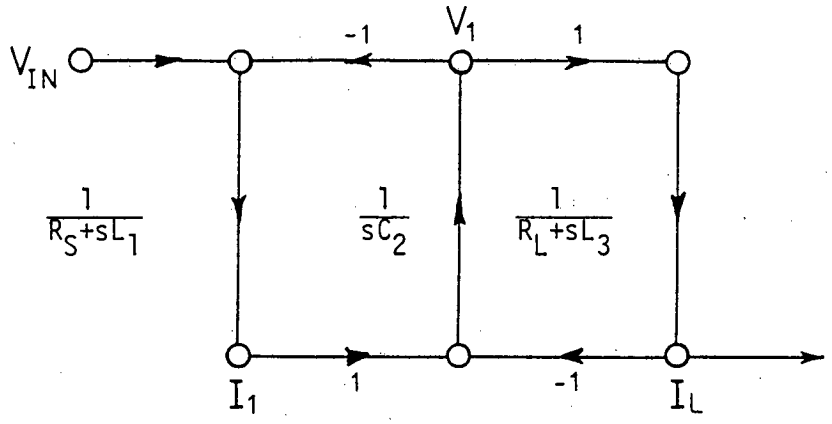


(b)

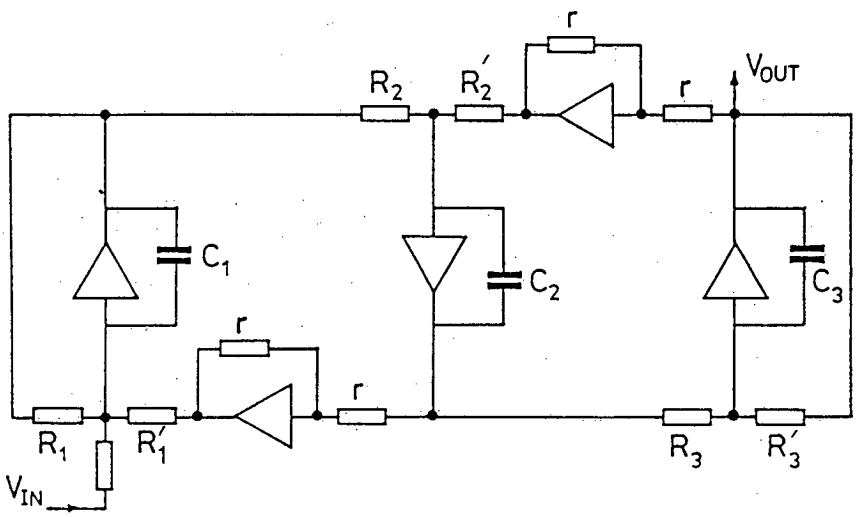
FIG.4.2: Active realisation of the passive, all-pole, lowpass ladder filters

(a) A third-order, doubly-terminated, all-pole, lowpass LC ladder filter.

(b) Block diagram of a possible active realisation of (a).



(c)



(d)

FIG.4.2: (continued)

(c) A signal flow graph representation of (a).

(d) Active realisation of (a), using integrators and summers.

then the transfer function $\frac{V_L'}{V_{IN}}$ (c.f. Fig. 4.2(b)) is proportional to H_{21} defined in Eqn (4.5). From Eqns (4.9) to (4.11) it is clear that transfer functions T_1, T_2 and T_3 may be obtained from differential integrators. Active simulation of RLC ladder filters, which contain integrators, summers and inverters, are called active ladder or leapfrog circuits, which was first introduced by Girling and Good in the early 70's[168]. Traditionally, the design of leapfrog filters starts from a block diagram called the signal flow graph, from which the final realisable, active circuit is obtained. An example of a signal flwo graph for Fig. 4.2(a) and its active realisation are shown in Figs. 4.2(c) and 4.2(d) respectively[22,168]. Since, in active ladder (or leapfrog) filters, integrator gain constants are proportional to the value of L or C in RLC ladder filters, i.e. there is direct correspondence between the integrator multiplier and the reactive elements, the resulting leapfrog filter retains the same minimum sensitivity as the passive prototype. This is the key property that attracts the attention of filter designers.

4.4 Sampled-Data Realisation of Active Leapfrog Circuits

In section 4.3 it was shown that it may be possible to design active inductorless filters, equivalent to low sensitivity resistively terminated LC filters, by employing differential integrators. Thus the low sensitivity of the original passive filter will be maintained by the equivalent active filter. Low sensitivity is not only desirable in active continuous filters, but also in other branches of filters the search has always been for low sensitivity structures. For example, in digital filters, highly accurate multipliers need longer word lengths for their coefficients, and from the hardware point of view, these multiplier coefficient word lengths should be

as small as possible. Therefore, if a digital filter is insensitive to its multiplier coefficients, then the realisation of its multipliers is much simpler. One of the early attempts to synthesise low sensitivity digital filters was made by Fettweis which ended in a very desirable filter called the Wave Digital Filter[170]. The basis of wave digital filter synthesis is the theory of unit elements and the analogy between a digital filter and a transmission line equivalent. Another successful approach to designing low sensitivity digital filters has been introduced by Bruton[171]. This approach is based on the analogy with the continuous active leapfrog structure in the voltage current domain rather than adopting the concepts of wave-filtering, adaptors, etc. In his approach to the realisation of low sensitivity digital ladder filters, Bruton has proposed several transformations to obtain discrete integrators including Direct-Transform Digital Integrator (DDI) and Lossless Discrete Integrator (LDI). Conventional SC ladder filters have benefited from Bruton's DDI and LDI transformations to some extent. In the next two sections these two transformations will be reviewed.

4.4.1 Direct-Transform Discrete Integrator (DDI) Transformation

The DDI as introduced by Bruton may be represented by the block diagram of Fig. 4.3(a). In this diagram the value of the multiplier is T/RX_i where T is the sampling period, R is the circuit normalising resistance, and X_i is the L or C element of the passive RLC prototype[171]. The switched-capacitor integrator having the same block diagram has been introduced by Hosticka[9]. This SC integrator has been derived from the well-known Miller integrator after replacing the resistor by a parallel switched-capacitor equivalent resistor (PER) described in Chapter 2. The Miller and switched-capacitor

integrators are shown in Figs. 4.3(b) and 4.3(c) for the purpose of comparison. A z-domain transfer function of the above SC integrator may be obtained from the continuous time integrator after replacing s by the following approximation:

$$s \equiv \frac{z-1}{T} \tag{4.12}$$

and by using the relationship of $R = T/C_R$ for the SC equivalent resistor. Thus, if the voltage transfer function of the continuous integrator shown in Fig. 4.3(b) is of the form:

$$H(\Omega) = \frac{-1}{sRC} \tag{4.13}$$

where $s = j\Omega$, then the sampled-data transfer function of the SC integrator shown in Fig. 4.3(c) is obtained as:

$$H(z) = \frac{(-C_R/C)z^{-1}}{1 - z^{-1}} \tag{4.14}$$

From Eqn (4.14) it is observed that the capacitor ratio (C_R/C) (equivalent to T/RX_i of Bruton's integrator) and the sampling time T are the only factors determining the integrator gain constant. Since the capacitor ratios in MOS integrated circuits can be controlled far better than the absolute values of individual capacitors and resistors, the SC integrators are superior to their active-RC counterparts. This is the main reason that SC integrators and the filter structures composed of SC integrators have received so much attention.

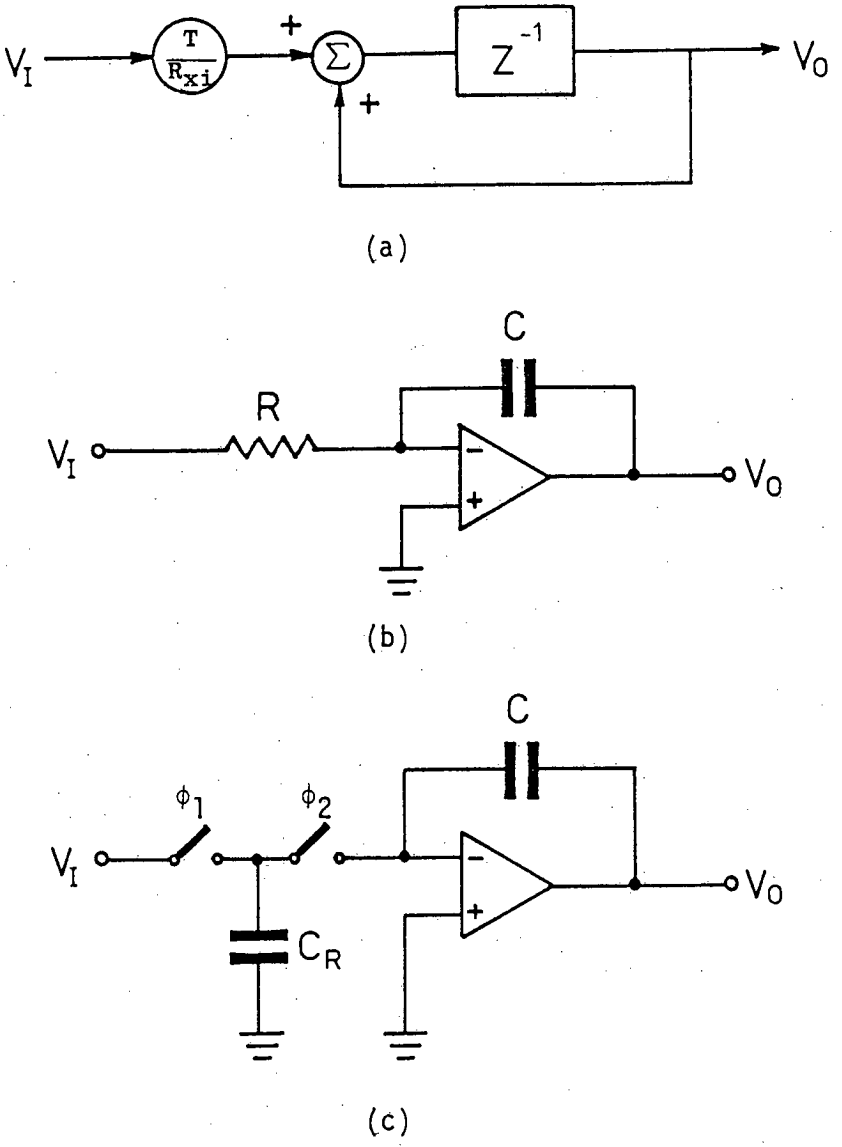


FIG.4.3: The switched-capacitor realisation of the direct-transform discrete integrator (DDI).

(a) Block diagram representation of the DDI.

(b) The Miller integrator.

(c) Switched-capacitor realisation of the DDI (and also the LDI).

Since, by applying the DDI transformation to an active ladder filter, the resulting SC ladder filter contained amplitude as well as phase errors, another transformation called the LDI transformation was adopted by designers of early SC ladder filters[15]. The LDI transformation which was originally proposed by Bruton[171] will be described in the next section.

4.4.2 Lossless Discrete Integrator (LDI) Transformation

The requirement for a discrete integrator to provide an absence of a delay-free forward path (to be realisable), and that its transfer function must ideally map onto the unit circle for $z = e^{j\omega T}$, lead to the following transformation which was first suggested by Bruton[171]:

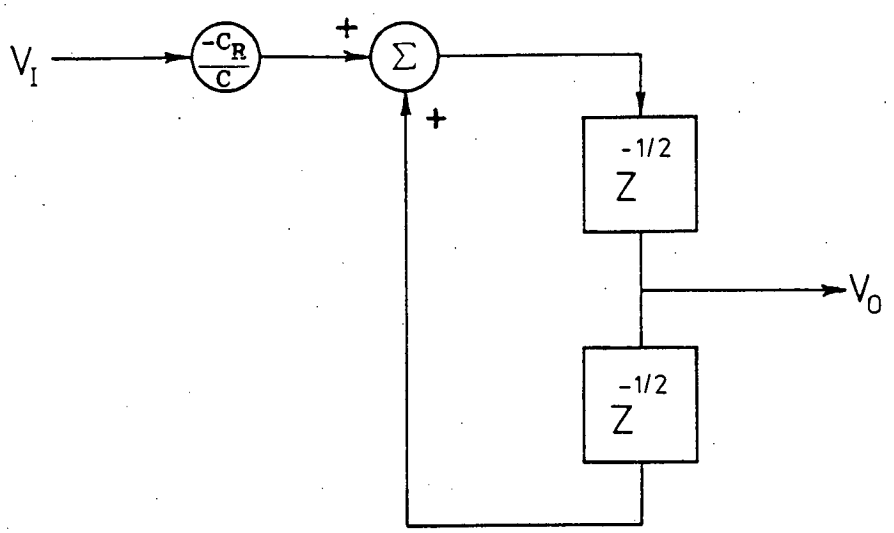
$$s \equiv \frac{1}{T} \cdot \frac{z-1}{z^{\frac{1}{2}}} = \frac{2}{T} \sinh\left(\frac{sT}{2}\right) \tag{4.15}$$

where T is the sampling time.

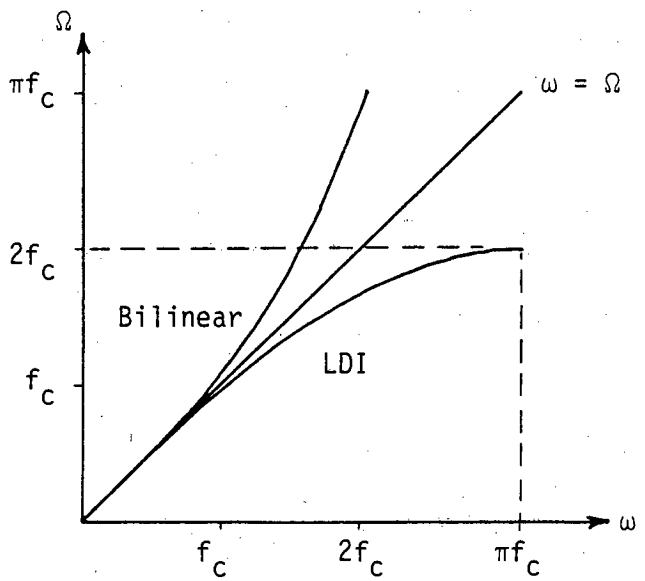
Eqn (4.15) represents the LDI transformation. A block diagram representation of the LDI is shown in Fig. 4.4(a), which should be compared with Fig. 4.3(a). It is easy to show that SC integrator shown in Fig. 4.3(c) represents both the DDI and the LDI transformations. For example, writing the charge equation for the SC integrator shown in Fig. 4.3(c) results in the following equation:

$$H(z) = \frac{V_0(z)}{V_i(z)} = \frac{(-C_R/C)\, z^{-\frac{1}{2}}}{1 - z^{-1}} \tag{4.16}$$

assuming that the output is sampled immediately after it is available[7,12-14]. By comparing Eqns (4.14) and (4.16) it is



(a)



(b)

FIG.4.4: The lossless discrete integrator (LDI) transformation.

(a) Block diagram representation of the LDI.

(b) Comparison between the bilinear and the LDI transformations.

observed that the only difference between the DDI and the LDI is the $z^{-\frac{1}{2}}$ delay term. For the reason given above, the SC integrator shown in Fig. 4.3(c) is generally known as the LDI transformation.

It is worthwhile to compare the LDI transformation with the Bilinear transformation reviewed in section 2.5.3, i.e.

$$s \equiv \frac{2}{T}\frac{z-1}{z+1} \tag{4.17}$$

In Chapter 2 it was mentioned that a desirable transformation from the s-plane to the z-plane should satisfy two basic requirements: namely, the imaginary axis of the s-plane should be mapped onto the unit circle of the z-plane, and also a stable continuous-time filter should map into a stable discrete-time filter. Both requirements are fulfilled by Bilinear and LDI transformations[169]. However, there are two significant differences between these transformations. The first difference is the different nature of the frequency warping introduced by each of the above transformations. For example, if we let $z = e^{j\omega T}$ in Eqn (4.16) we obtain:

$$s = j\frac{2}{T}\sin\frac{\omega T}{2} \tag{4.18}$$

Then after substituting $j\Omega$ for s in the continuous domain, the following relation results:

$$\Omega = \frac{2}{T}\sin\frac{\omega T}{2} \tag{4.19}$$

where Ω is the continuous-time frequency and ω is the discrete-time frequency.

The counterpart of Eqn (4.19) for the bilinear transformation was given in Eqn (2.22) which is repeated for simplicity:

$$\Omega = \frac{2}{T} \tan \frac{\omega T}{2} \tag{4.20}$$

The difference between the two warping effects is shown in Fig. 4.4(b).

The second difference between the bilinear transformation and LSI transformation is that the former maps the entire s-plane imaginary axis $j\Omega$ ($-\infty$ to $+\infty$) onto the z-plane unit circle, while the latter maps a finite section of the $j\Omega$ axis ($-\frac{2}{T} \leq \Omega \leq \frac{2}{T}$) onto the z-plane unit circle.

A serious drawback of the LDI transformation is creating improper terminations for the SC ladder filters. This point will be described in the next section.

4.4.3 SC Ladder Terminations

Application of the LDI transformation to the doubly terminated ladder networks is equivalent to multiplying all the prototype ladder elements by the factor $z^{-\frac{1}{2}}$ (= exp ($-j\omega T/2$)) including the termination resistances[172]. It has been shown[173-175] that each of the resulting terminations is equivalent to a frequency-dependent resistor in parallel with a frequency-dependent reactance element. This will affect the low sensitivity of the SC filter and poses distortion[77]. The distortion in filter response becomes more serious as the ratio of passband edge to the sampling frequency becomes larger, thus hindering the usage of the SC filters for high-frequency applications.

By using the exact analysis and synthesis of the above mentioned SC ladder filter due to Scanlan[17], the problems resulting from the improper terminations are overcome, and the limitation of high clock rates is removed. Exact design of the SC lowpass ladder filter is described in the next section for the case of a third-order all-pole lowpass filter, shown in Fig.4.5.

4.5 Exact Design of Switched-Capacitor All-Pole Lowpass Ladder Filters

The analysis given in this section is based on Scanlan's approach[17]. Details of the experimental validation of this analysis for a third-order, maximally flat, all-pole lowpass ladder filter realised as an NMOS integrated circuit are given in Chapter 6.

4.5.1 Exact Analysis

By inspecting Fig. 4.5, it is observed that there are only two types of SC integrators which construct the whole SC lowpass ladder filter. First a lossless SC integrator without feedback switched-capacitors, shown in Fig. 4.6(a). Secondly, a lossy SC integrator with feedback switched-capacitor to simulate the input and output terminations, shown in Fig. 4.6(b). Note that, although a third-order filter is shown in Fig. 4.5, any higher order lowpass ladder filter may be obtained by including more lossless SC integrators in the circuit, bearing in mind that the total number of the integrators (or operational amplifiers) should be equal to the order of the filter.

Exact analysis of the sampled-data lossless integrator shown in Fig. 4.6(a), results in the following charge equation:

$$C_B V_3(nT) = C_B V_3[(n-1)T] + C_A V_1[n-\tfrac{1}{2})T] - C_A V_2[(n-\tfrac{1}{2})T] \qquad (4.21)$$

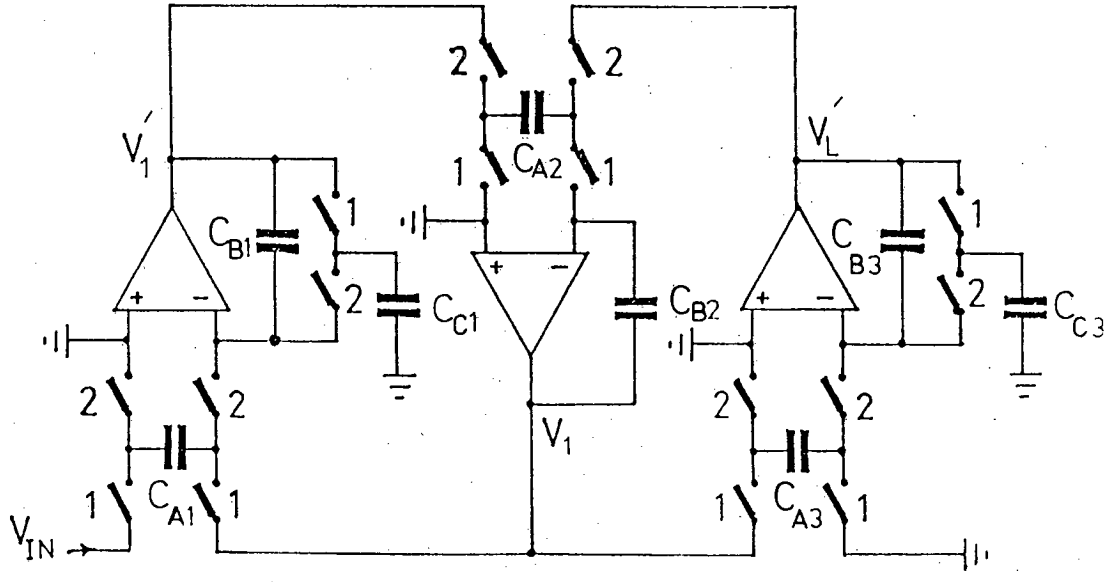


FIG.4.5: Circuit diagram of the experimental, switched-capacitor third-order, all-pole, lowpass ladder filter.

assuming an ideal operational amplifier, and that samples of the output voltage are taken at times $t = mT$ while the capacitor C_A is switched to the input voltage at times $t = (m+\frac{1}{2})T$ and switched to the operational amplifier inputs at $t = mT$.

Taking the z-transform ($z = e^{sT}$) and after some algebraic manipulation we obtain:

$$V_3(z) = \frac{z^{-\frac{1}{2}} [V_1(z) - V_2(z)]}{\frac{C_B}{C_A}(1-z^{-1})} = \frac{V_1(z) - V_2(z)}{2\frac{C_B}{C_A} \sinh (sT/2)} \tag{4.22}$$

where $s = j\omega$, $\sinh (sT/2) = (e^{sT/2} - e^{-sT/2})/2$, and T is the sampling time.

For the second integrator shown in Fig. 4.6(b) with the same assumptions, we obtain the following charge equation:

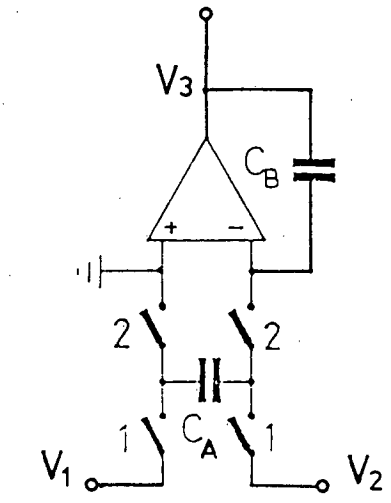
$$C_B V_3(nT) = C_B V_3[(n-1)T] + C_A V_1[(n-\tfrac{1}{2})T] - C_A V_2[(n-\tfrac{1}{2})T] - C_C V_3[(n-1)T] \tag{4.23}$$

Then by taking the z-transform and after some algebraic manipulation:

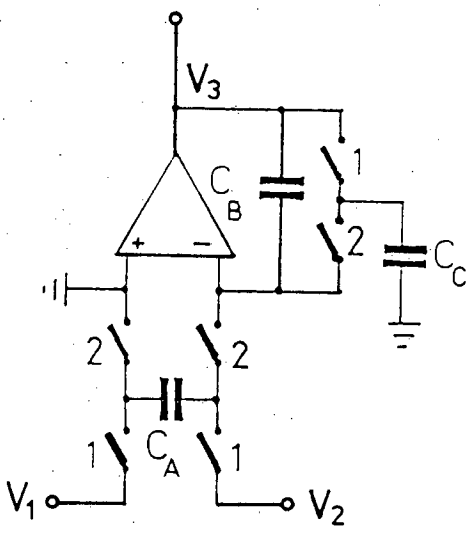
$$V_3(z) = \frac{V_1(z) - V_2(z)}{\frac{C_B}{C_A}(z^{\frac{1}{2}} - z^{-\frac{1}{2}}) + \frac{C_C}{C_A} z^{-\frac{1}{2}}}$$

$$= \frac{V_1(z) - V_2(z)}{\frac{2C_B - C_C}{C_A} \sinh (sT/2) + \frac{C_C}{C_A} \cosh (sT/2)} \tag{4.24}$$

where s, T and $\sinh (sT/2)$ were defined above and $\cosh (sT/2) = (e^{sT/2} + e^{-sT/2})/2$.



(a)



(b)

FIG.4.6: Switched-capacitor lossless (a), and lossy (b) integrators.

If for simplicity we put:

$$\gamma = \sinh(sT/2)$$

$$\mu = \cosh(sT/2)$$

$$\lambda = \frac{\gamma}{\mu} = \tanh(sT/2) \qquad (4.25)$$

Eqns (4.22) and (4.24) may be briefly described by the following equations:

$$V_3 = \frac{V_1 - V_2}{k\gamma} \qquad \text{(for lossless integrators)} \qquad (4.26)$$

and

$$V_3 = \frac{V_1 - V_2}{k_1\gamma + k_2\mu} \qquad \text{(for lossy integrators)} \qquad (4.27)$$

Comparing Eqn (4.27) with Eqn (4.11) or (4.9), reveals that, in contrast to the passive RLC ladder filter, the simulated SC ladder filter has frequency dependent terminations, because the second term in the denominator of Eqn (4.27) contains μ which is frequency dependent (c.f. Eqn (4.25)).

It should now be clear that the transfer functions T_1, T_2 and T_3 shown in Fig. 4.2(b), when realised by SC integrators have the following general forms:

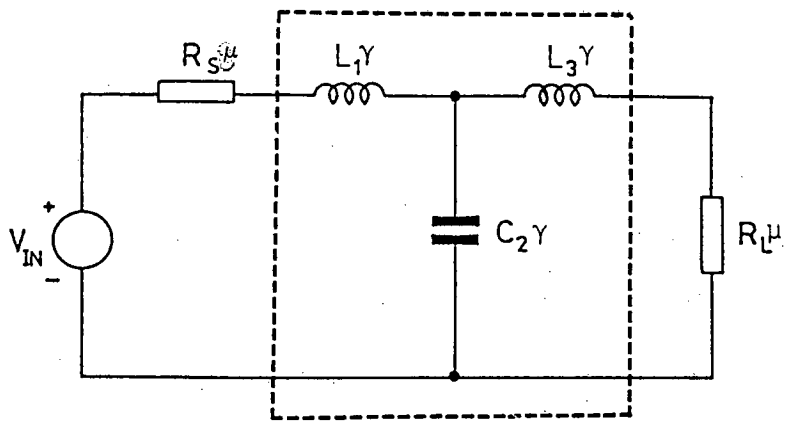
$$T_1 = \frac{1}{k_1\gamma + k_1'\mu} \qquad (4.28)$$

$$T_2 = \frac{1}{k_2\gamma} \qquad (4.29)$$

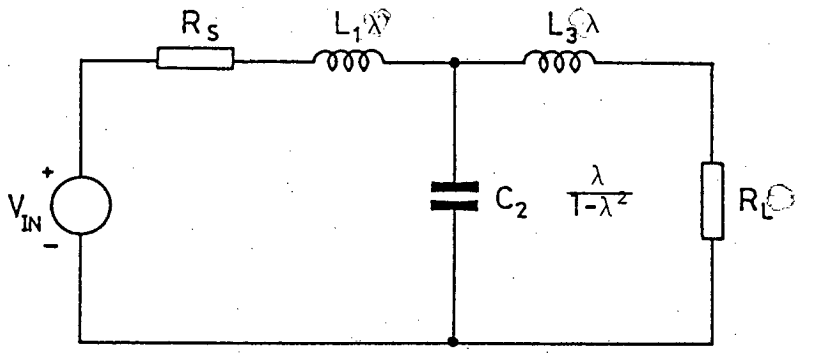
and $$T_3 = \frac{1}{k_3\gamma + k_3\mu} \qquad (4.30)$$

Now the overall transfer function of the SC ladder filter shown in Fig. 4.5, may be obtained by comparing Fig. 4.2(a) with 4.2(b), keeping in mind that T_1, T_2 and T_3 are defined by Eqns (4.28) to (4.30). In the derivation, the equivalent circuit of Fig. 4.7(a) is obtained which is the result of the exact analysis of SC integrators. In other words, the transfer function of Fig. 4.7(a), viz: I_L/V_{IN}, is the same as that of Fig. 4.5, (V_L/V_{IN}) if the inductors and capacitors have the values shown in Fig. 4.7(a), and if the frequency variable is γ rather than s. Thus to analyse or synthesise the SC network of Fig. 4.5, it is only necessary to consider the equivalent circuit of Fig. 4.7(a). The established analysis and synthesis methods may be applied to the circuit of Fig. 4.7(a), because by remembering that for $s = j\omega$, $\gamma = \sinh(sT/2) = j \sin(\omega T/2)$ and $\mu = \cosh(sT/2) = \cos(\omega T/2)$, this circuit is a lossless two-port terminated in real resistors, although frequency dependent ($R_S\mu$ and $R_L\mu$). In section 4.4.3, it was mentioned that the existence of frequency dependent terminations is undesirable in the approximate design of SC ladder filters. But from the stability point of view, they are rather necessary because if the terminations R_L and R_S were achieved in the realisation then the denominators of $H_{21}(\gamma)$ would contain only left-half plane roots in γ (with all L and C positive). Now the left-half roots in γ produce both right- and left-half plane roots in s and so the filter would be unstable[66, 171].

The transfer function of the circuit shown in Fig. 4.7(a), $H_{21}(\gamma)$, may be obtained by multiplying the ABCD matrices[176] belonging



(a)



(b)

FIG.4.7: Equivalent networks for the exact analysis and synthesis of the switched-capacitor filter shown in Fig.4.5.

to the LC network (separated by dashed lines), and the source termination, i.e.

$$\begin{bmatrix} V_{IN} \\ I_1 \end{bmatrix} = \begin{bmatrix} \mathcal{E} & R_S\mu \\ 0 & 1 \end{bmatrix} \begin{bmatrix} A(\gamma) & B(\gamma) \\ C(\gamma) & D(\gamma) \end{bmatrix} \begin{bmatrix} V_L \\ I_L \end{bmatrix} \tag{4.31}$$

where $V_L = I_L R_L \mu$

and $$\begin{bmatrix} A(\gamma) & B(\gamma) \\ C(\gamma) & D(\gamma) \end{bmatrix} = \begin{bmatrix} 1 & L_1\gamma \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ C_2\gamma & 1 \end{bmatrix} \begin{bmatrix} 1 & L_3\gamma \\ 0 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1+L_1C_2\gamma^2 & (L_1+L_3)\gamma + L_1C_2L_3\gamma^3 \\ C_2\gamma & 1 + C_2L_3\gamma^2 \end{bmatrix} \tag{4.32}$$

Thus

$$H_{21}(\gamma) = \frac{I_L}{V_{IN}} = \frac{1}{R_L\mu A(\gamma)+R_S\mu D(\gamma)+B(\gamma)+R_SR_L\mu^2C(\gamma)}$$

$$= \frac{1}{R_L\mu(1+L_1C_2\gamma^2)+R_S\mu(1+C_2L_3\gamma^2)+(L_1+L_3)\gamma+L_1C_2L_3\gamma^3+R_SR_LC_2\gamma\mu^2} \tag{4.33}$$

Although the above information given for the equivalent circuit of Fig. 4.7(a) is sufficient for the exact synthesis given in the next section, by scaling the components of Fig. 4.7(a), (by μ), some interesting results are obtained which are as follows. Firstly, all the reactances L and C will be functions of λ instead of γ, where $\lambda = \mu/\gamma = \tanh(sT/2)$ which is more convenient for use in analysis and synthesis, because [176].

$$\lambda = j\Omega \qquad \text{for } s = j\omega$$

$$\mathrm{Re}(\lambda) \gtrless 0 \qquad \text{for Re } s \gtrless 0$$

Secondly, after the above-mentioned impedance scaling an equivalent circuit is obtained which has frequency independent termination and is analogous to the cascade of (n-1) transmission line unit elements together with a single zero of transmission at infinity as is described by Scanlan[17]. This analogy helps the designer to choose the proper transfer function for the later synthesis. This point will be clear in the next section.

Now from the circuit point of view, impedance scaling is performed by including two ideal transformers of the ratio $\mu^{-\frac{1}{2}}$ and $\mu^{\frac{1}{2}}$ before and after the LC network, respectively. This is equivalent to dividing all the inductors by μ, and multiplying all capacitors by μ in the circuit of Fig. 4.7(a). The resulting circuit is shown in Fig. 4.7(b), which has the following transfer function:

$$H'_{21} = \frac{I_L}{V_{IN}} = \frac{1}{R_L A(\gamma)+R_S D(\gamma)+\frac{1}{\mu}B(\gamma)+R_S R_L \mu C(\gamma)}$$

$$= \frac{1}{R_L(1+L_1C_2\gamma^2)+R_S(1+C_2L_3\gamma^2)+(L_1+L_3)\frac{\gamma}{\mu}+L_1C_2L_3\frac{\gamma^3}{\mu}+R_sR_L\mu C_2\gamma} \qquad (4.34)$$

which is equivalent to:

$$H'_{21} = \mu H_{21} = (1-\lambda^2)^{-\frac{1}{2}} H_{21} \qquad (4.35)$$

where μ and λ were defined in Eqn (4.35), and H_{21} was given by Eqn (4.33).

In the next section, from the information obtained by the analogy between the equivalent circuit of Fig. 4.7(b) and the cascade of unit elements, a proper transfer function is chosen. This transfer function is then synthesised using the well-established Darlington procedure[177] to calculate the element values of the equivalent of the circuit of Fig. 4.7(a). Finally, the capacitor ratios of the individual integrator in the SC ladder filter shown in Fig. 4.5 are obtained by comparing Eqns (4.9) to (4.11) with those given in Eqns (4.22) to (4.24).

4.5.2 Exact Synthesis

From the analogy between the auxiliary network of Fig. 4.7(b), and the cascade of transmission line unit elements mentioned in the previous section, it is implied that the transfer function $H_{21} = I_L/V_{IN}$ of the equivalent circuit of Fig. 4.7(a), must be of the form[178]:

$$H_{21}(\lambda) = \frac{(1 - \lambda^2)^{n/2}}{Pn\ (\lambda)} \tag{4.36}$$

where λ has already been defined by Eqn (4.25); n is the number of unit elements; and, Pn (λ) must be a Hurwitz polynomial[177] in the variable λ to guarantee the stability of the realised network, which in our case is a switched-capacitor circuit. Then from Eqn (4.35) and Eqn (4.36) it is concluded that:

$$H'_{21}(\lambda) = \frac{(1 - \lambda^2)^{(n-1)/2}}{Pn\ (\lambda)} \tag{4.37}$$

Then the synthesis proceeds by forming:

$$\left|H'_{21}\right|^2 = \frac{\left|S_{21}\right|^2}{4R_L R_S} \tag{4.38}$$

for the auxiliary circuit of Fig. 4.7(b) $\left|S_{21}\right|^2$ is the transducer power gain of Fig. 4.7(b), and S_{21} is an element of scattering matrix[179] which is very useful in networks where power flow is a prime consideration, e.g. filters.

Although it is possible to continue the synthesis by the usual techniques of unit element extraction as described by Scanlan[17], in the following, a simplified synthesis approach suggested by Baher et al[180] is adopted to obtain the capacitor ratios of the realised SC ladder filter shown in Fig. 4.5 which was implemented in this research. The simple example of a third-order, maximally flat, all-pole lowpass filter is given because all the synthesis steps could be performed analytically and hence the main aspects of the synthesis procedure are revealed. Note that in the following example, the termination resistors are normalised to the value of 1Ω for simplicity. However, the network components may be scaled by any desired factor for any particular requirement, for example, to change the voltage (or power) gain of the network.

One possible form of Eqn (4.36), for which the maximally flat solution exists is:

$$\left|H_{21}\ (j\Omega)\right|^2 = \frac{K}{1 + \left(\frac{\sin\theta}{\eta}\right)^{2n}} \tag{4.39}$$

Therefore the transfer function $H_{21} = I_L/V_{IN}$ belonging to the equivalent circuit of Fig. 4.7(a), must be of the form shown in Eqn (4.39), in which $K = \frac{1}{4}$ for 1Ω terminations; $n = 3$ the order of the filter; $\eta = \sin(\omega_o T/2) = \sin(\pi f_o/f_s) = \sin(\pi/8.28) = 0.37$;

$\Omega = \tan(\omega T/2) = \tan\theta$; $\omega_o = 2\pi f_o$ is the 3-dB point; and $T = \frac{1}{f_s}$ is the sampling period, as usual.

The transfer function H_{21} defined in Eqn (4.39) is also the transfer function of cascaded n unit elements.

The next step is to obtain $\left|S_{21}\right|^2$ from Eqns (4.35) and (4.38). This results in:

$$\left|S_{21}\right|^2 = \frac{\cos^2\theta}{1 + \left(\frac{\sin\theta}{0.37}\right)^6} \tag{4.40}$$

Then the reflection coefficient S_{11} is calculated from Eqn (4.40) and the following equation:

$$\left|S_{11}\right|^2 = 1 - \left|S_{21}\right|^2 \tag{4.41}$$

which results in the following, after assigning the left-half λ-plane poles and zeros to $S_{11}(\lambda)$[180]:

$$S_{11}(\lambda) = \frac{\lambda \prod_{r=1}^{2} \left(\sqrt{1-(0.37)^3\exp(j2\psi_r)}\right) \lambda - j(0.37)^{3/2}\exp(j\psi_r)}{\prod_{r=1}^{3} \left(\sqrt{1-(0.37)^2\exp(j2\phi_r)}\right) \lambda - j(0.37)\exp(j\phi_r)} \tag{4.42}$$

where $\phi_r = \frac{2r-1}{2n}\pi$

$$\psi_r = \frac{2r-1}{2(n-1)}\pi$$

and n is the order of the filter.

After some algebraic manipulation $S_{11}(\lambda)$ is obtained as:

$$S_{11}(\lambda) = \frac{1.0012899\lambda^3 + 0.3369399\lambda^2 + 0.0508096\lambda}{1.0012898\lambda^3 + 0.7717475\lambda^2 + 0.293546\lambda + 0.0508096} \quad (4.43)$$

Next, the input impedance of the auxiliary network in Fig. 4.7(b) is determined from[179]:

$$Z'_{IN} = \frac{1 + S_{11}}{1 - S_{11}} \quad (4.44)$$

Hence

$$Z'_{IN} = \frac{q_3\lambda^3 + q_2\lambda^2 + q_1\lambda + q_0}{p_2\lambda^2 + p_1\lambda + p_0} \quad (4.45)$$

where:

$q_3 = 2.0025796$

$q_2 = 1.1086874$

$q_1 = 0.3443556$

$q_0 = 0.0508096$

and

$p_2 = 0.434807$

$p_1 = 0.247364$

$p_0 = 0.0508096$

From the input impedance of the auxiliary network in Fig. 4.7(b), the input impedance of the equivalent circuit shown in Fig. 4.7(a) will be obtained, because the capacitor values of the realised SC ladder network in Fig. 4.5 must be obtained from the equivalent

circuit in Fig. 4.7(a) and not from the auxiliary network in Fig. 4.7(b)[17]. Thus by using Eqn (4.45):

$$Z_{IN} = \mu Z'_{IN} = \frac{\mu(q_3\lambda^3 + q_2\lambda^2 + q_1\lambda + q_0)}{p_2\lambda^2 + p_1\lambda + p_0}$$

$$= \frac{(q_3+q_1)\gamma^3+\mu(q_2+q_0)\gamma^2+q_1\gamma+\mu q_0}{(p_2+p_0)\gamma^2+\mu p_1\gamma+p_0} \qquad (4.46)$$

where the relations $\lambda = \gamma/\mu$ and $\mu^2 = (1 + \gamma^2)$ have been employed to arrive at the final result. Finally, from Eqns (4.45) and (4.46), Z_{IN} is obtained as:

$$Z_{IN} = \frac{23469.35\gamma^3 + 11594.97\mu\gamma^2 + 3443.55\gamma + 508.09\mu}{4856.17\gamma^2 + 2427.36\gamma\mu + 508.09} \qquad (4.47)$$

By performing the continued fraction expansion[179] of Z_{IN} around $\gamma = \infty$, the element values of the equivalent circuit in Fig. 4.7(a) are obtained as:

$$L_1 = 4.83H$$

$$C_2 = 4.91F \qquad (4.48)$$

and $$L_3 = 1.94H$$

assuming $R_S = R_L = 1\Omega$.

Finally, the capacitor ratios for the individual integrators in the SC ladder network of Fig. 4.5 are determined using the above component values and also Eqns (4.22) and (4.24). Thus, for the first lossy integrator (see Fig. 4.6(b)):

$$L_1 = 2\frac{C_{B1}}{C_{A1}} - \frac{C_{C1}}{C_{A1}}$$

$$4.83 = 2\frac{C_{B1}}{C_{A1}} - 1 \qquad \text{where } \frac{C_{C1}}{C_{A1}} = R_S = 1$$

and $$\boxed{\frac{C_{B1}}{C_{A1}} = 2.91} \tag{4.49}$$

For the lossless integrator (see Fig. 4.6(b)):

$$C_2 = \frac{2C_{B2}}{C_{A2}}$$

$$4.91 = 2\frac{C_{B2}}{C_{A2}}$$

thus $$\boxed{\frac{C_{B2}}{C_{A2}} = 2.45} \tag{4.50}$$

Finally, for the last integrator (lossy):

$$L_3 = 2\frac{C_{B3}}{C_{A3}} - \frac{C_{C3}}{C_{A3}}$$

$$1.94 = 2\frac{C_{B3}}{C_{A3}} - 1 \qquad \text{where } \frac{C_{C3}}{C_{A3}} = R_L = 1$$

therefore

$$\boxed{\frac{C_{B3}}{C_{A3}} = 1.47} \tag{4.51}$$

Note that in the above calculation, for simplicity,

$C_{A1} = C_{A2} = C_{A3} = C_{C1} = C_{C3}$.

Using the above capacitor ratios, the SC lowpass ladder network in Fig. 4.5 was realised in NMOS integrated form. Details of the design considerations and experimental results are given in Chapters 5 and 6.

4.6 Comparison Between the Exact and the Approximate Designs

From Eqn (4.39) the transfer function of the SC third-order lowpass ladder filter given as an example for the exact design, may be obtained as:

$$\left|H_{21}\right|^2 = \frac{\frac{1}{4}}{1 + 334\sin^6\theta} \tag{4.52}$$

In the approximate design in which a very large sampling frequency is assumed, the element values for the prototype passive

network are obtained from the standard tables[181]. In that case

$$L_1 = L_2 = \frac{1}{\eta}$$

and $$c = \frac{2}{\eta}$$

where $$\eta = \frac{\omega_o \pi}{\omega_s} \tag{4.53}$$

Now if the above values of L's and c are substituted in Eqn (4.33), after some algebraic manipulation, the following transfer function is obtained for the approximate design:

$$\left|H_{21}\right|^2 = \frac{\frac{1}{4}}{1 - \sin^2\theta + (1 - \eta^2)^2 \frac{\sin^6\theta}{\eta^6}} \tag{4.54}$$

which in the case of our example ($\eta = 0.37$) reduces to:

$$\left|H_{21}\right|^2 = \frac{\frac{1}{4}}{1 - \sin^2\theta + 246 \sin^2\theta} \tag{4.55}$$

It is clear that the response given by Eqn (4.55) is the distorted version of the response obtained from Eqn (4.52) which belonged to the exact design. The two frequency responses for the exact and approximate designs are compared in Fig. 4.8.

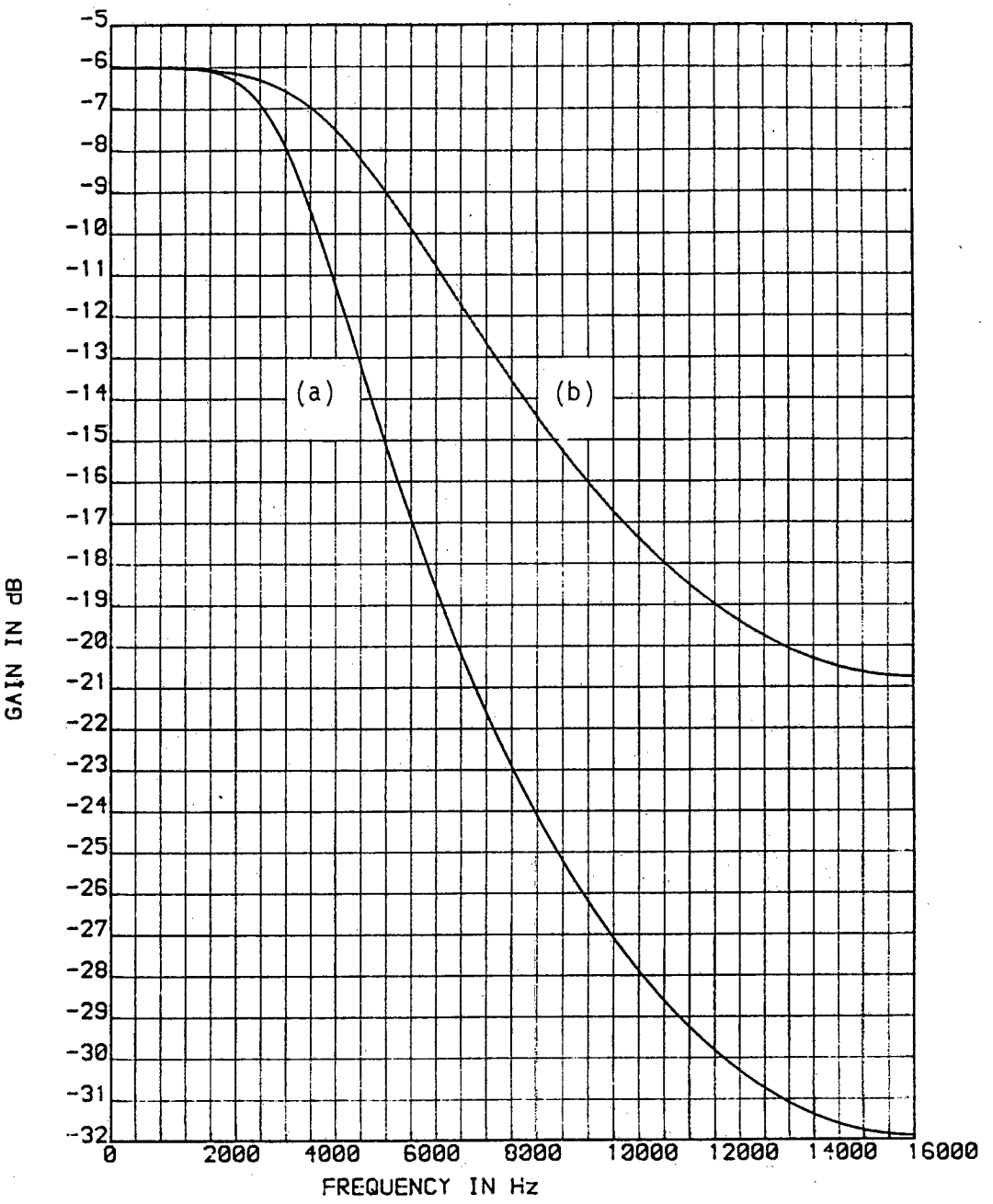


FIG.4.8: Simulated comparison between the frequency responses of the switched-capacitor filter shown in Fig.4.5, applying the exact (a) and the approximate (b) designs.

CHAPTER 5: PRACTICAL DESIGN CONSIDERATIONS FOR SWITCHED-CAPACITOR LADDER FILTER REALISATION

5.1 Introduction

In the analysis and synthesis of the SC lowpass ladder filter discussed in Chapter 4, it was assumed that the passive and active components of the filter, viz, switches, capacitors and operational amplifiers, were ideal. This is not the actual case, indeed, as the realised components in MOS integrated circuits have practical limitations. Limitations of MOS components and non-idealities will affect the realised filter performance to a greater or lesser extent. For example, the non-zero "on" resistance of the MOSFET switches, impose a limitation on the maximum clock frequency to which the SC filter can operate. It also contributes to the total r.m.s. noise of the filter. The stray capacitances associated with both MOS transistor switches and MOS capacitors affect the frequency response accuracy of the SC filter and increase its total harmonic distortion. Finally, the non-ideal behaviour of MOS operational amplifiers will contribute to the noise, distortion and frequency response deviation of the filter.

In the following sections, a brief description of SC filter elements in integrated form, along with their practical limitations, will be given. Also their significant effects on the SC filter performance will be studied through analysis or computer simulation. It will be shown that most of the non-ideal effects are so small that they can usually be ignored. Those which cannot be ignored, can be minimised or compensated for by careful integrated circuit layout.

5.2 MOS Transistor Switches

The MOS transistor makes an almost ideal electronic analogue switch, combining a high channel conductance in the "on" state with a low leakage current in the "off" state. Further, there is a good d.c. isolation between the switching and signal waveforms and the transistor will pass signals with negligible offset over a range almost as large as that of the switching waveform.

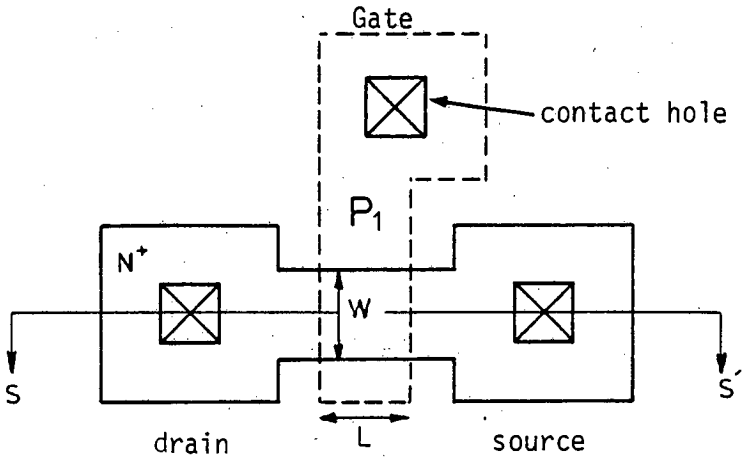
Switches used in SC filters can be made from a single, minimum size, MOS enhancement transistor. This point will be justified in the next section. The top and side views of a typical silicon gate NMOS enhancement transistor are shown in Fig. 5.1. This layout was actually employed in the final realisation of the experimental SC ladder filter (Chapter 6).

5.2.1 Charging Characteristics of a Minimum Size MOS Transistor

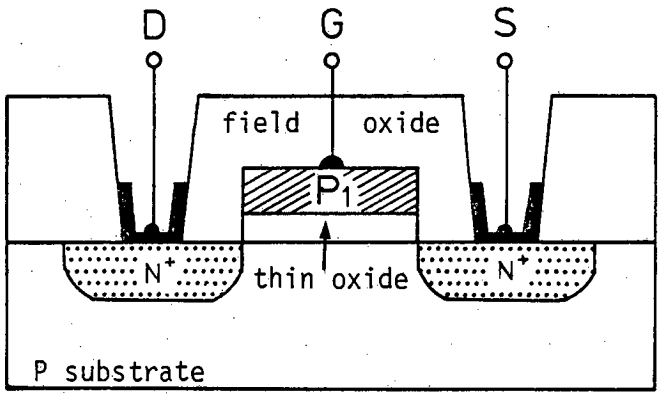
When a capacitor is charged through an MOS transistor switch, the time taken to settle within a prescribed percentage of the final value may be obtained from the following expression[182], (see also Fig. 5.2):

$$T_{on} \simeq \frac{C}{\beta_o \left(\frac{W}{L}\right)} \quad \frac{1}{V_\phi - V_T - V_H} \log_e \left(\frac{1}{2k}\right) \tag{5.1}$$

where C is the value of the capacitor, β_o is the MOS transistor process gain factor, W and L are width and length of the MOS transistor (shown in Fig. 5.1(a)) respectively, V_ϕ is the applied gate voltage, V_T is the threshold voltage of the MOS transistor (including the "body effect"), V_H is the input voltage, and k is the settling tolerance. Substituting the typical values (see for



(a)

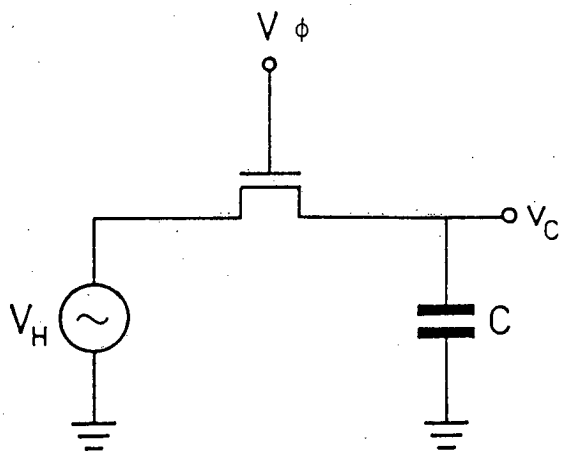


(b)

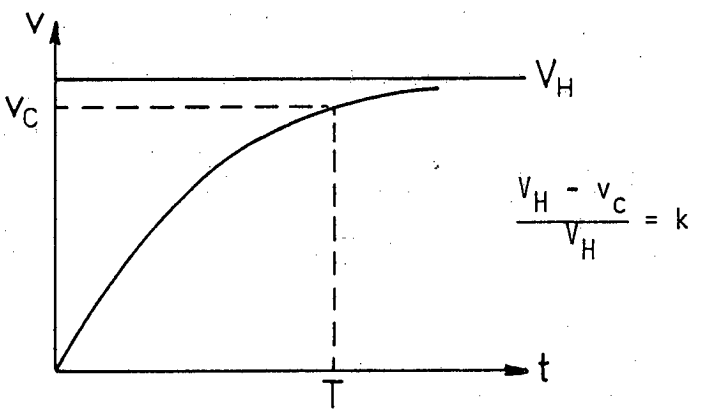
FIG.5.1: MOS transistor implementation

(a) Layout (not to scale)

(b) Cross section at SS'



(a)



(b)

FIG.5.2: MOS switched-capacitor charging time

(a) charging of a capacitor by an MOS transistor switch.

(b) Exponential charging curve defining the variables in Eqn 5.1.

example, Appendix C) for above coefficients in Eqn (5.1), viz, β_o = 25 μA/V², W/L = 1 (transistor aspect ratio), V_ϕ = 15 V, V_T = 1.25 V, V_H = 10 V, k = 0.1 per cent, and using the maximum capacitor employed in the experimental SC filter (C = 20 pF), the value of T_{on} is obtained as one microsecond (μsec.). If the clock pulse that turns the switch "on" has a duty cycle of 33%, its pulse duration is 10 μsec. for a clock frequency of 32 kHz. This time is at least 10 times T_{on} calculated from Eqn (5.1). Therefore, the minimum size MOS transistors (W/L = 1), can safely be used as charge switches in the experimental SC filter.

5.2.2 "ON" Resistance of the MOS Transistor Switches

The finite (non-zero) resistance of an MOS transistor (MOST) switch limits the rate at which charge is transferred through an SC circuit. The value of this resistance which becomes important at high clock rates could be found from the following relation[183]:

$$R_{on} = [\beta_o \frac{W}{L} (V_{GS} - V_T)]^{-1} \qquad (5.2)$$

where β_o, W, L, and V_T have been defined in the previous section and V_{GS} is the gate-to-source voltage. Eqn (5.2) indicates that the "on" resistance of MOS transistor switches is voltage dependent, and hence variable. A value as high as 5 kohms has been reported[7] for the "on" resistance of minimum size MOS transistor switches.

Since the SC lowpass ladder filter described in Chapter 4 is formed by the inter-connection of SC integrators, it is useful to investigate the effect of finite "on" resistance of the MOST switches on the gain of the SC integrator shown in Fig. 5.3(a).

Assuming an ideal operational amplifier, during the sampling interval ϕ_1, the charging network can be represented as the series $R_{on}C_R$ combination shown in Fig. 5.3(b)[167]. The voltage V_c across the capacitor C_R at the end of the sampling interval ϕ_1, in response to the input voltage of ΔV_{in} is:

$$V_c(t_1) = \Delta V_{in} (1 - e^{-t_1/R_{on}C_R}) \tag{5.3}$$

where t_1 is the "on" time of ϕ_1. The charge on C_R after t_1 is:

$$Q_c(t_1) = C_R V_c (t_1) = C_R \Delta V_{in} (1 - e^{-t_1/R_{on}C_R}) \tag{5.4}$$

During the integration phase, ϕ_2, the operational amplifier transfers the charge from C_R to C as shown in Fig. 5.3(c). The voltage on C_R after the integration interval, t_2, is:

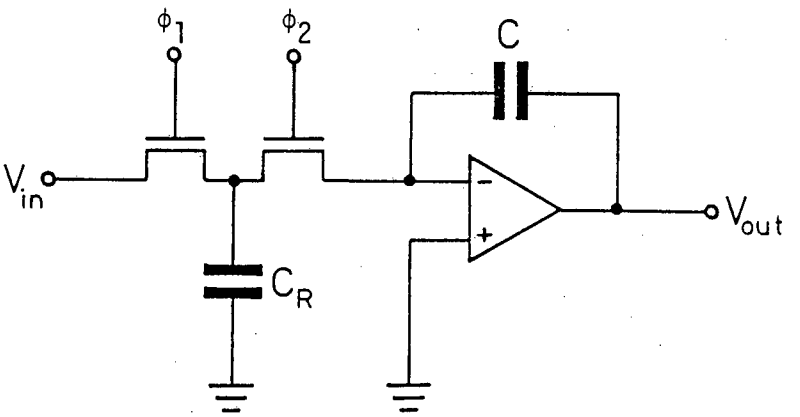
$$V_c(t_2) = V_c(t_1) e^{-t_2/R_{on}C_R} \tag{5.5}$$

with a charge of

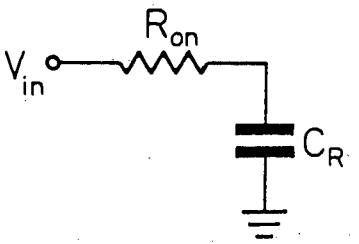
$$Q_c (t_2) = C_R V_c (t_2) = C_R V_c (t_1) e^{-t_2/R_{on}C_R} \tag{5.6}$$

Assuming a 50% duty cycle clock, i.e. $t_1 = t_2 = t$, the total change in the charge of the capacitor C_R during one complete clock cycle is given by:

$$\begin{aligned} \Delta Q_c &= Q_c (t_1) - Q_c (t_2) \\ &= C_R \Delta V_{in} (1 - e^{-t/R_{on}C_R})^2 \end{aligned} \tag{5.7}$$



(a)



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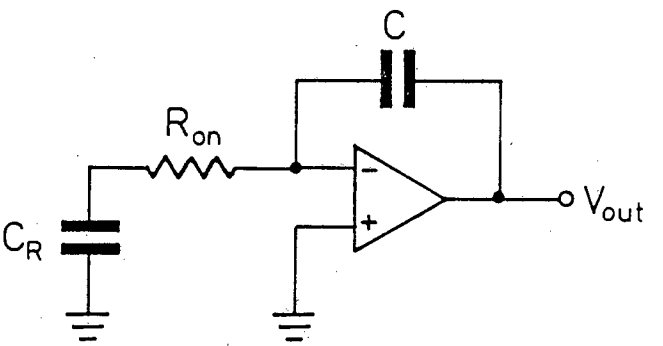


(c)

FIG.5.3: RC time constants formed by the "on" resistance of the MOS transistor switches and the capacitors in a switched-capacitor integrator (a), during the two non-overlapping clock phases ϕ_1 (b), and ϕ_2 (c).

Since $\Delta V_{out} = -\frac{\Delta Q_C}{C}$, the integrator gain is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = -\left(\frac{C_R}{C}\right)\left(1 - e^{-t/R_{on}C_R}\right)^2 \qquad (5.8)$$

Hence the non-zero switch resistance results in the incomplete transfer of charge, which is equivalent to a capacitor ratio error given by Eqn (5.8). From this equation it could be concluded that in order to keep the above capacitor ratio error less than 0.1%, the ratio $t/R_{on}C_R$ should be more than 7.6. As mentioned earlier, in the SC lowpass ladder filter, realised in integrated form, the above ratio was more than 10. Therefore the capacitor ratio error due to "on" resistance of MOST switches could be ignored. Switching noise of the switched-capacitors resulting from "on" resistance of MOSFET switches is presented in section 5.5.

The "off" resistance of the MOST switch is many meg-ohms and the leakage current is so small that it can be neglected in the prototype. This is particularly so because the junction areas for a unity aspect ratio (W/L = 1) MOS transistors are of minimum size. This should ensure good performance at high temperatures, bearing in mind the fact that leakage currents in silicon devices approximately double for each 10 degrees Kelvin rise in temperature[183].

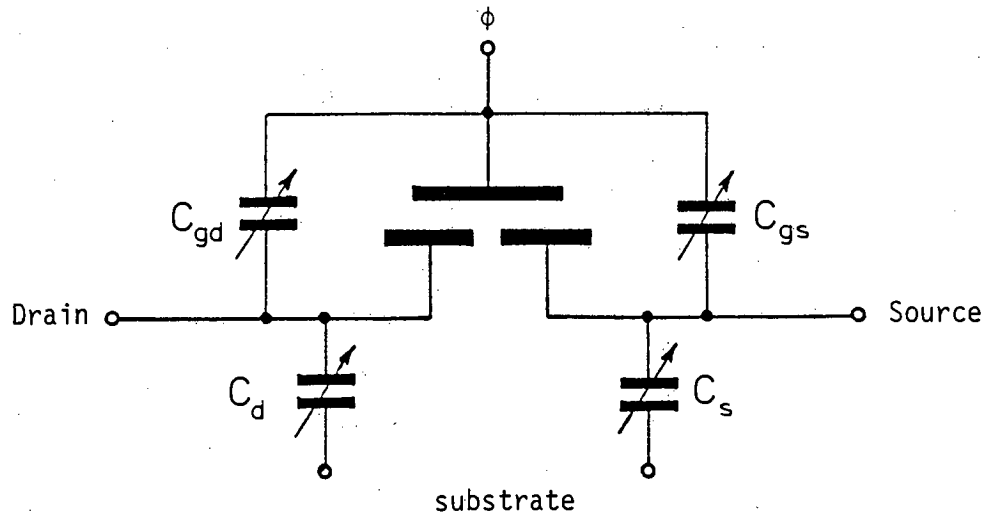
5.2.3 P-N Junction and Gate-Overlap Capacitances of MOS Transistor Switches

P-N junction and gate-diffusion capacitances of MOST switches will affect the SC filter performance, i.e. they contribute to the output noise, offset, harmonic distortion of the filter, as will be

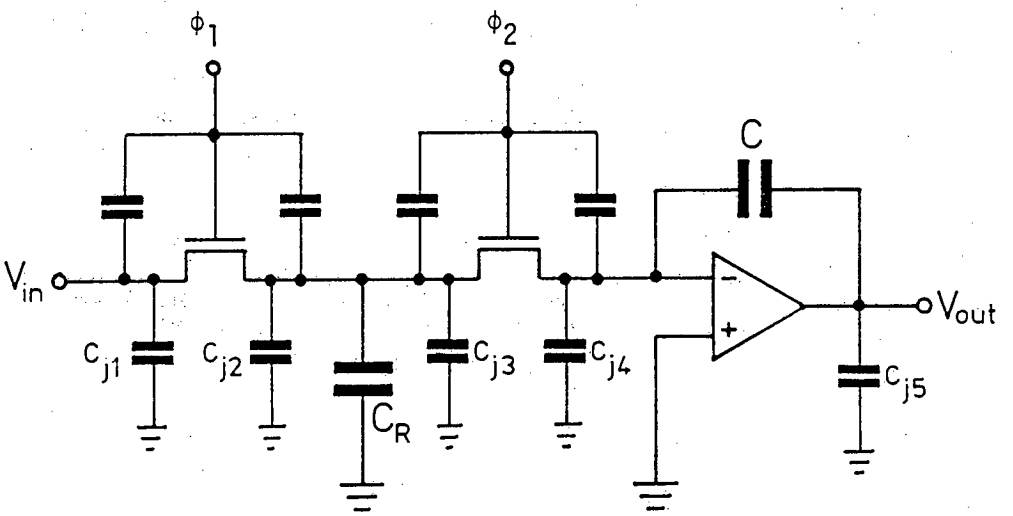
described later. These "stray" capacitances, which are voltage dependent, are shown in Fig. 5.4(a).

Gate-to-source and gate-to-drain (overlap) capacitances (C_{gs} and C_{gd}) and also P-N junction capacitances C_s and C_d are shown in Fig. 5.4(b), when associated with the MOST switches of a simple SC integrator. These stray capacitances can contribute to the degradation of the output signal in two ways. Firstly, they provide a path for the clock noise to be superimposed on the signal. The clock feedthrough can be decreased by lowering the clock voltage, and by using smaller gate-channel overlap. Since the MOST switches in our SC filter were fabricated by self-aligned silicon gate techniques (no gate-diffusion overlap), the clock feedthrough effects were almost completely eliminated. Secondly, they introduce dc offset[4]. It has been shown[184] that this dc offset could be up to $C_o V_\phi/(C_R + C)$ for the integrators shown in Fig. 5.4(b), where C_o is the channel capacitance of the MOST and V_o is the clock voltage.

Junction capacitances C_d and C_s, shown in Fig. 5.4(a), are the significant sources of non-linearity in any SC circuit. They add a large non-linear stray capacitance to the capacitor nodes connected to the MOST switch. Fig. 5.4(b) shows the junction capacitances associated with both sides of MOST switches. A more rigorous treatment of all stray capacitances in the differential SC integrator used in our SC ladder filter will be given in section 6.5. Among the stray capacitances identified in Fig. 5.4(b), only C_{j2} and C_{j3} are significant, because C_{j1} simply shunts the input voltage source, C_{j4} is at virtual ground, and C_{j5} is voltage driven.



(a)



(b)

FIG.5.4: Parasitic capacitances associated with a single MOS transistor switch (a), and in a parallel switched-capacitor integrator (b).

The change of capacitor ratios, i.e. filter coefficients, due to the junction capacitances C_{j2} and C_{j3} can be verified by realising that these stray capacitances appear in parallel with the switched-capacitor C_R. Thus

$$\Delta\alpha = \frac{C_R + C_{j2} + C_{j3}}{C} - \frac{C_R}{C} \approx \frac{2C_j}{C} \qquad (5.9)$$

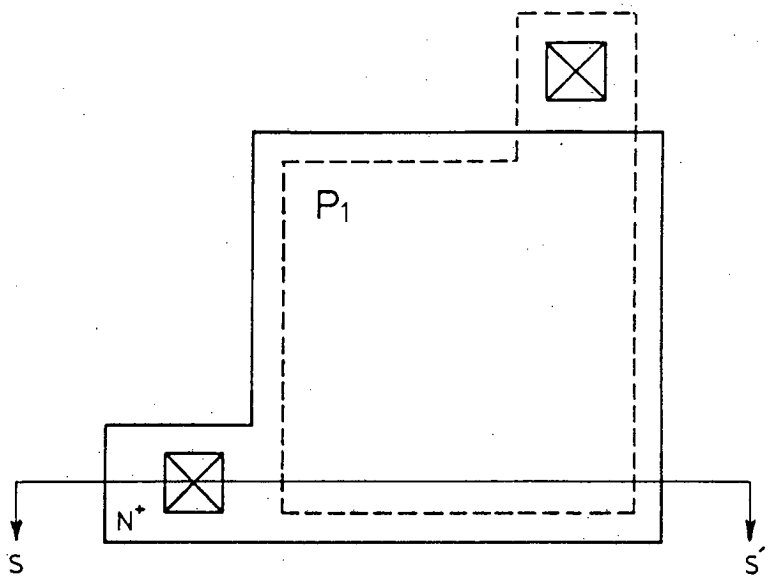
where $\Delta\alpha$ is the change in capacitor ratios or equivalently the change in the signal gain of the SC integrator.

From Eqn (5.9) it can be observed that the effect of the junction capacitance C_j is to change the capacitor ratios. More importantly, because of voltage dependence[185], it introduces a non-linear stray capacitance which results in the increased harmonic distortion of the SC filter. The measured harmonic distortion of the experimental SC lowpass ladder filter, realised in integrated form, will be given in Chapter 6.

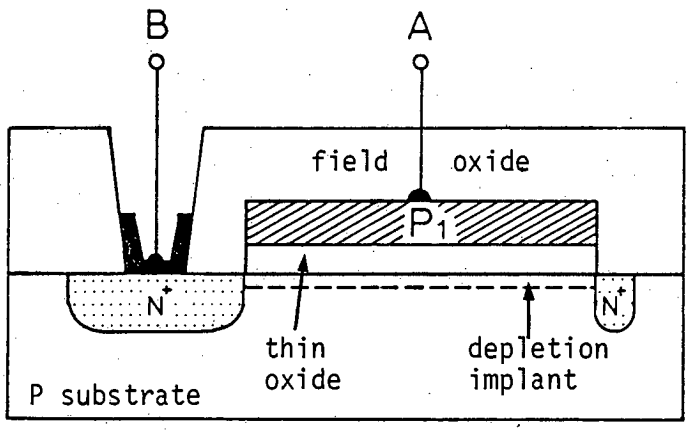
5.3 MOS Capacitors

Fig. 5.5 shows the top and side views of a polysilicon 1-oxide-diffusion capacitor used in the prototype integrated SC filter. This type of MOS capacitor is formed very similarly to an MOS transistor. However, for the normal operation of the capacitor, it is preferable that the threshold voltage be negative, and therefore the bottom capacitor plate receives the normal depletion implant in an enhancement-depletion MOS process.

In the following sub-sections, the non-idealities associated with the MOS capacitors, i.e. MOS capacitor mismatch, voltage and



(a)



(b)

FIG.5.5: MOS Capacitor implementation.

(a) Layout (not to scale).

(b) Cross section at SS'.

N.B. A to be biased positive relative to B.

temperature dependence, and the parasitic capacitances of the top and bottom plates of MOS capacitors will be described.

5.3.1 MOS Capacitor Mismatch

The capacitance for MOS capacitors is given by the usual parallel plate formula[186]:

$$C = C_{ox} A_c = \frac{\kappa_o \varepsilon_o A_c}{t_{ox}} \qquad (5.10)$$

where C_{ox} is the oxide (SiO_2) capacitance per unit area; A_c is the area of the top plate (P_1); κ_o is the relative dielectric constant of SiO_2 oxide; ε_o is the permittivity of free space; and t_{ox} is the oxide thickness.

Assuming that the dielectric constant ($\kappa_o \varepsilon_o$) and its thickness (t_{ox}) do not vary, the ratio of two capacitors made within the same integrated circuit will depend only on their area ratio. The geometrical shape of the capacitors is defined by the photolithographic mask[7] used to make the integrated circuit.

Because of the wavelength of the light used in photolithography and for other reasons including the poor control of the etching process, capacitor edge variation occurs. Thus the definition of the capacitor area is subject to random processing variation. This error could be minimised by increasing the capacitor areas and making square capacitors instead of rectangular or other shapes[4].

During the etching phase of the photomask process, a poorly controlled lateral etch occurs, called "undercut", which affects

the capacitor ratio definition. To overcome this problem a capacitor geometry should be used such that, the perimeter lengths (total length around the active area) as well as the areas are ratioed. For example, by paralleling identical square capacitors to form the larger capacitors[187], the capacitor ratios will not be affected by undercut.

Another factor which affects the capacitor ratio accuracy is the long range gradients of the capacitor oxide[4], which arise from non-uniform oxide growth conditions. The error from this source can be minimised by improved oxide growth techniques and by a common centroid geometry[36]. This may be achieved by locating the unit square capacitors in such a way that they are symmetrically spaced about a common centre point.

In general, the ratio accuracies achievable in practice range from 1-2 per cent for small capacitor geometries ($\sim$ 400 μm^2) to about 0.1 per cent for capacitor geometries which approach the limit of economic size (40,000 μm^2)[7].

As mentioned in Chapter 4, the passive LC ladder filters have minimum passband sensitivity to their passive element variations. It means that a small variation in the individual components does not cause a significant change in the passband response of the ladder filter. This property is preserved in SC ladder filters in which there is a direct correspondence between the passive (LC) elements of the prototype passive filter and the gain constants of the SC integrators. Since these gain constants are determined by capacitor ratios and the clock frequency assuming a stable clock, any change in

the capacitor ratios would cause the integrators' gain constants to change. To investigate the passband variation of the SC lowpass ladder filter (shown in Fig. 4.5), as a result of the capacitor ratio error in the individual integrators, the SCNAP programme was used (Appendix A). Capacitor ratios of the individual integrators were decreased by 1 per cent and it was observed that the capacitor ratio error of the first SC integrator was the main contributor to the slight change of the SC lowpass ladder filter's passband. Fig. 5.6 shows the passband variation of the abovementioned filter, as a result of 1 per cent decrease in the capacitor ratio of the first SC integrator. As it is seen in this figure, firstly the sensitivity of the SC lowpass ladder filter is almost zero at the frequencies where the maximum output gain occurs (from dc to 300 Hz), secondly the maximum change in the passband is only 0.006 dB, which demonstrates the expected low sensitivity of the SC ladder filters.

5.3.2 Temperature and Voltage Dependence of MOS Capacitors

A great advantage of the SiO_2 dielectric used in implementing MOS capacitors is its very low temperature coefficient of approximately 20 ppm/^oC[6], in contrast with approximately 2000 ppm/^oC for diffused resistors and several hundred ppm/^oC for thin film and implanted resistors. The above mentioned temperature coefficient is much less for the capacitor ratios. In fact, if the temperature-dependent MOS capacitance value could be linearly approximated about a nominal temperature, it is easy to show that the MOS capacitance ratio is almost independent of temperature.

The voltage dependence of a capacitor C, may be characterised by[4]:

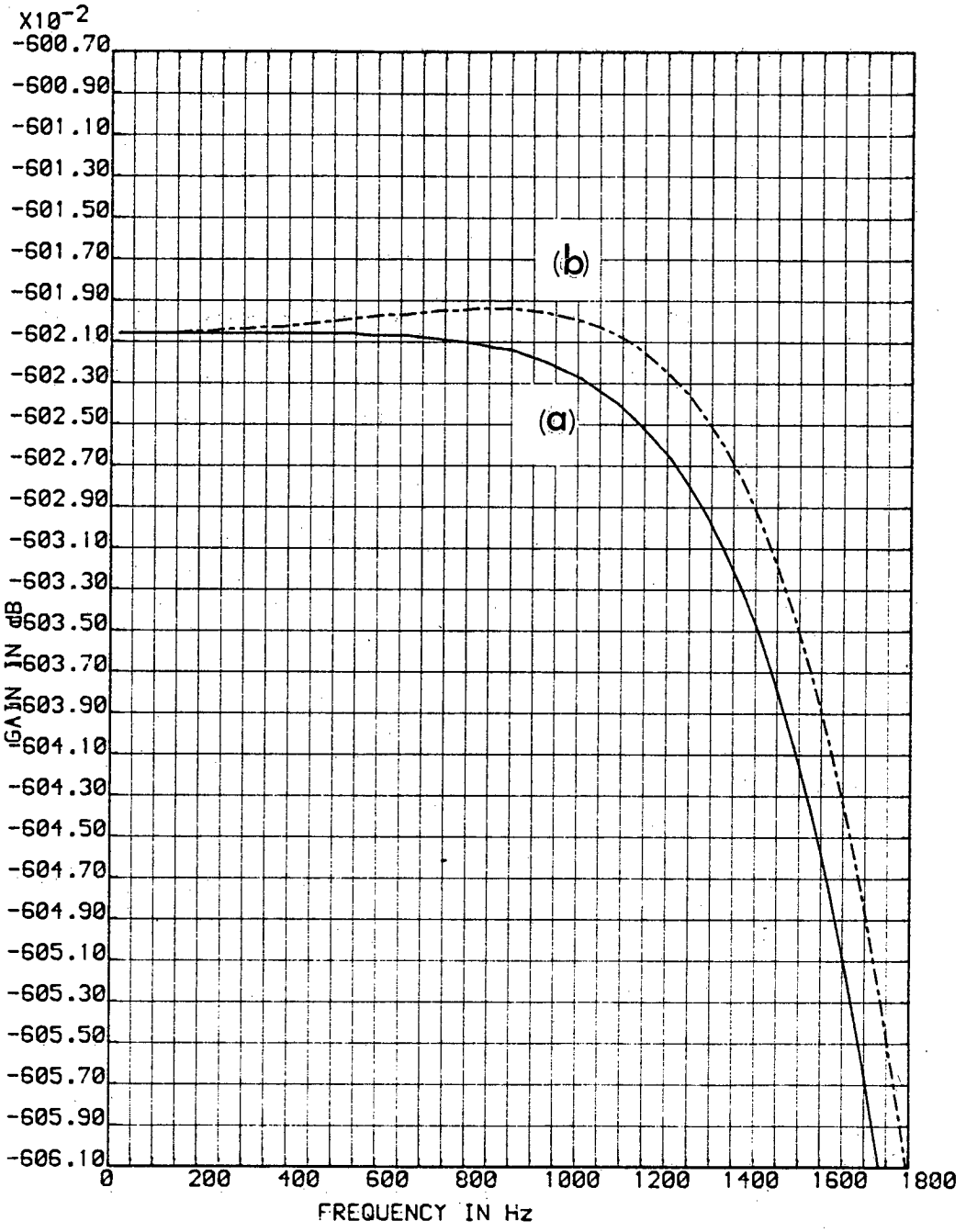


FIG.5.6: Simulated passband responses of the switched-capacitor lowpass ladder filter shown in Fig.4.5, with the nominal values (a), and with one per cent decrease in the capacitor ratios of the first (most sensitive) integrator (b).

$$\nu = \frac{1}{C}\frac{\partial C}{\partial V} \tag{5.11}$$

where ν is the effective voltage coefficient of the MOS capacitor. In the case of a simple SC integrator (e.g. Fig. 5.3(a)), the voltage dependence of MOS capacitors C_R and C, expressed about a nominal operating voltage, V_0, can be given as:

$$C_R(V_{in}) = C_R(V_0)\,[1 + \nu\,(V_{in} - V_0)] \tag{5.12}$$

and

$$C(V_{out}) = C\,(V_0)\,[1 + \nu\,(V_{out} - V_0)] \tag{5.13}$$

In some capacitor structures, e.g. metal over n^+, or a polysilicon layer capacitor, the voltage coefficient, ν, is very small, in the order of 10 ppm/volt[189]. However, capacitors which employ a single layer of polycrystalline silicon (including the capacitor structure shown in Fig. 5.5), have a higher voltage dependence, typically in the order of 100 ppm/volt[6]. Clearly, the resulting effect is the increase in total harmonic distortion of the SC filter. Thus, care should be taken in designing the capacitor structures for SC filters. Different MOS capacitor structures have been reviewed by Hodges[189].

5.3.3 Parasitic Capacitances

There are non-linear stray capacitances associated with both plates of MOS capacitors. The size of these stray capacitances depends on the particular capacitor structure used. In general, the stray capacitance associated with the bottom plate is much bigger (5-20%) compared to the top plate stray capacitance (0.1 - 1%)[7]. The effect of these stray capacitances is to deviate the

frequency response of the SC filter from its nominal one, and to increase the total harmonic distortion. Thus, every attempt should be made to eliminate, compensate for or at least minimise the effects of stray capacitances by designing stray-insensitive circuits and by choosing large capacitor sizes, whenever possible. A general method of designing SC stray-insensitive circuits comprising only integrators was presented in Chapter 3.

5.4 MOS Operational Amplifiers

Operational amplifiers are necessary elements in large-scale integrated (LSI) analogue circuits such as sampled-data and switched-capacitor filters. Compared to bipolar transistor technology, MOS yields matched pairs of transistors with an order of magnitude higher offset voltage, an order of magnitude lower gain per stage, and much higher noise, particularly to the 1/f component[189]. Thus MOS amplifiers do not compete with their bipolar transistor counterparts. Nevertheless, the MOS amplifiers are three to five times smaller in area than their bipolar counterparts, and they are technologically compatible[6].

In the following sub-sections, the important parameters of MOS operational amplifiers from the standpoint of SC filters will be reviewed.

5.4.1 Finite Gain and Bandwidth Effects

The most important limitation of practical operational amplifiers used in integrated analogue filters is their modest, frequency dependent gain. This may be defined as[148]:

$$A(s) = \frac{A_o \omega_c}{s+\omega_c} \qquad (5.14)$$

assuming an operational amplifier with a dominant pole. In Eqn (5.14), A_o is the dc open-loop gain of the operational amplifier, ω_c is the corner frequency of its frequency response, and s is the usual Laplace operator. The term $A_o.\omega_c$ is called the "gain-bandwidth product" of the operational amplifier, which is usually quoted in specifications.

The effects of finite gains and bandwidths of operational amplifiers on the performance of SC integrators and SC biquad filters have already been studied analytically[190-192]. Particularly, in the case of a single stage SC integrator, it has been shown that it is the dc open loop gain of operational amplifiers which dominates the performance.

The effects of operational amplifier finite gain and bandwidth on the frequency of SC lowpass ladder filter shown in Fig. 4.5 , (and the subject of Chapters 4, 5 and 6) were studied in this research, using the SCNAP programme. The results are shown in Figs. 5.7 and 5.8. These figures show that the finite gain of operational amplifiers results in a significant loss in the passband of the SC filter. Also the finite bandwidth of operational amplifiers introduces frequency peaking near the cut-off frequency. Therefore both finite gain and finite bandwidth effects could significantly restrict the performance of the SC ladder filter. The SCNAP predictions have been experimentally confirmed, and are presented in Chapter 6.

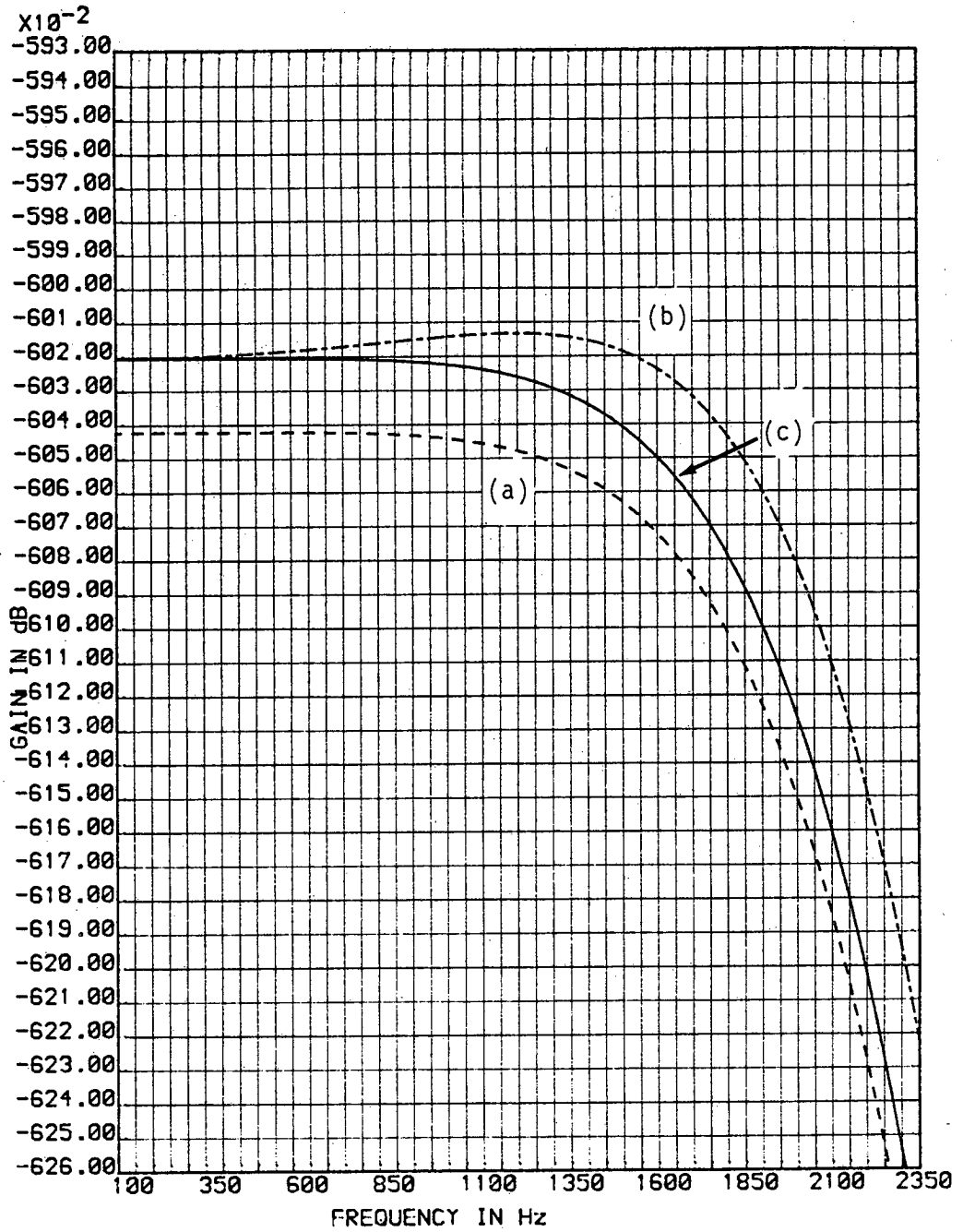


FIG.5.7: Simulated effects of the operational amplifier finite gain (a) and bandwidth (b) on the passband response of the switched-capacitor filter shown in Fig.4.5. Response (c) is the passband of the filter with the nominal values.

N.B. Operational amplifier gain in (a) was 1000.
Operational amplifier bandwidth in (b) was 1MHz.

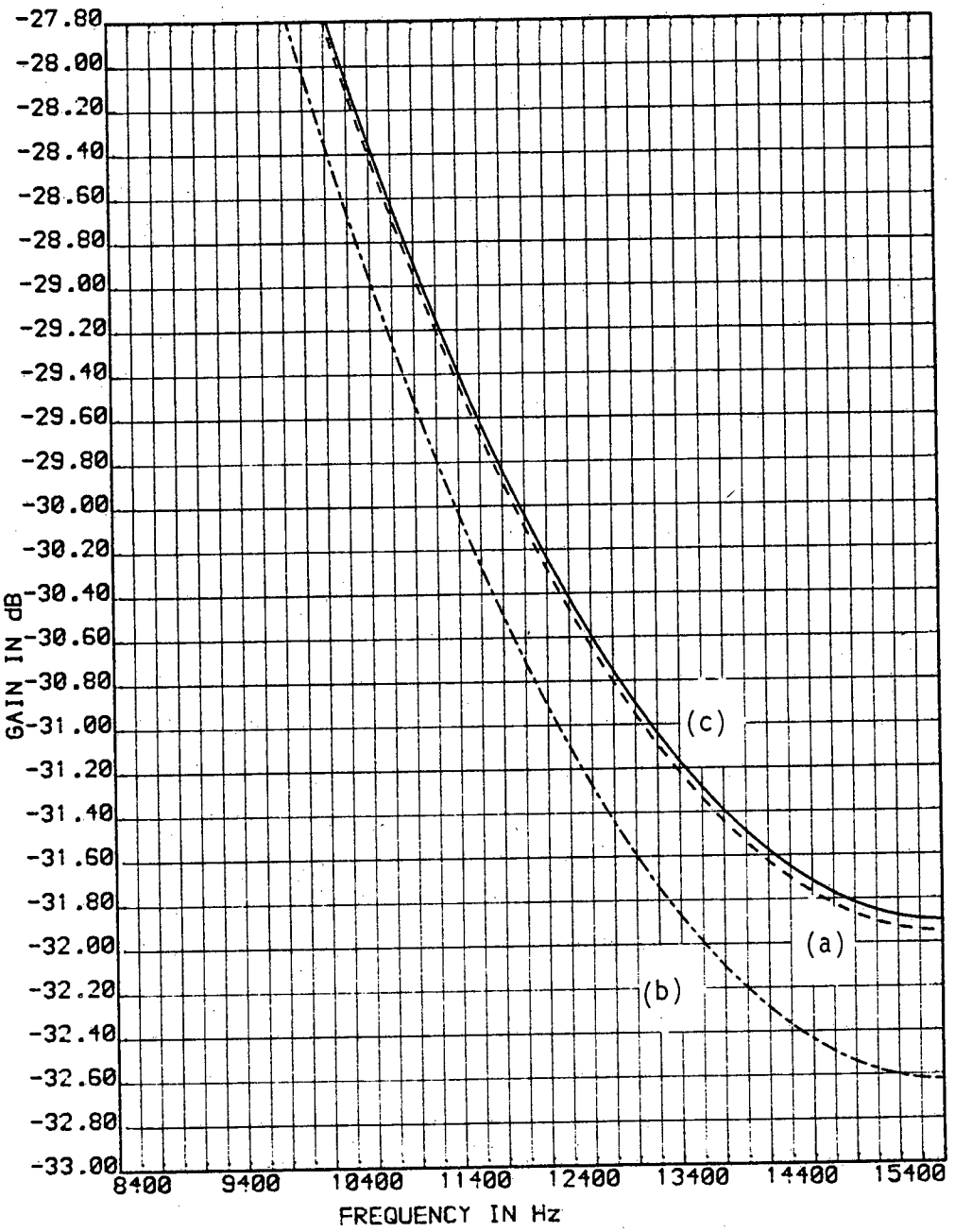


FIG.5.8: Simulated effects of the operational amplifier finite gain and bandwidth on the attenuation band of switched-capacitor filter shown in Fig. 4.5. Curves (a), (b) and (c) have been defined in Fig.5.7.

5.4.2 Slew-Rate and Settling Times

The response time of an operational amplifier to a step input is determined by its slew-rate and settling time. However, in designing MOS operational amplifiers, the gain and phase margins must take priority for stability considerations. Therefore the slew rates are largely predetermined[193].

Since the operational amplifiers in the SC lowpass ladder filters considered in this research, are connected as integrators, they only need to respond to the signal changes once every clock cycle. Therefore the slew-rate requirement depends on the sampling rate of the SC filter, i.e. it is more relaxed for lower clock frequencies.

Slew-rate limiting is caused by some capacitor associated with the operational amplifier (usually the compensation capacitor) that cannot be charged or discharged fast enough. This suggests that small capacitor values should be used for faster operation of SC filters. Therefore the exact designs of SC filters such as those described in Chapter 4 in which low capacitor ratios can be used, provide a means of extending the useful range of the SC filter to several hundred kHz.

The settling time is commonly specified as the time required for step response to settle within certain percent of the final value[151]. Under typical conditions, the operational amplifier used in our SC filter settled to within 1 mV in 2 μsec in response to a 2.5 V step. This time is 600 nsec for 1 V steps. In general,

the settling time is the main consideration in determining the maximum sampling frequency for an SC filter[194,195]. In section 6.7 the experimental results of the effects of high clock frequencies on the frequency response of the SC lowpass filter are presented.

Noise of operational amplifiers will be discussed in the next section.

5.5 Noise Sources

There are three main sources of noise in SC filters[7,34,196-201], namely: thermal noise of MOST switches, flatband thermal noise of operational amplifiers, and finally 1/f or flicker noise of operational amplifiers, which dominates all other noise at low frequencies (ignoring sampling effects).

When an MOS transistor switch is turned "on" connecting a capacitor C_R (see Fig. 5.3(b)) to a voltage source, the thermal noise power density in the resistance channel of the switch, $4\ kT\ R_{on}$[7], appears in series with the voltage source. This noise is bandlimited by the RC circuit formed by the "on" resistance of the switch (R_{on}), and the sampling capacitor (C_R). This single-pole lowpass circuit has a noise bandwidth of $1/(4\ R_{on}C_R)$[202]. Thus the bandlimited noise power is:

$$V^2_{r.m.s.} = (4\ kT\ R_{on})\left(\frac{1}{4\ R_{on}C_R}\right) = \frac{kT}{C_R} \qquad (5.15)$$

where k = Boltzmann's constant, and T = temperature in ^oK. When the "KTC" noise is sampled and held in the SC filter, the resulting noise includes the duty cycle (τ) of the clock and other

sampling effects, as it is derived by Fischer[201], i.e.

$$S_c(f) = \frac{kT}{f_s.C_R} \cdot (1-\tau)^2 \left(\frac{2B_{eq}}{f_s}\right).\text{sinc}^2 \left(\frac{(1-\tau)f}{f_s}\right) \qquad (5.16)$$

where $S_c(f)$ is the output noise spectral density of the switched capacitor; B_{eq} is the equivalent noise bandwidth, ($= 1/(2R_{on}.C_R)$ for double sided spectrum); f_s is the sampling frequency, and $\text{sinc } x = \frac{\sin \pi x}{\pi x}$. Eqn (5.16) predicts some useful information about the noise in SC filters. For example, it shows that there is a direct relation between the output noise and the ratio of B_{eq}/f_s. It also shows that the longer the duty cycle the smaller the noise. Finally, the (sin x)/x envelope provides effective anti-alias filtering.

For the present MOS transistor sizes and capacitors in the range of picofarads, the noise bandwidth is a few megahertz (MHz), in the "on" state. Therefore, according to Eqn (5.16), the sampled noise of the switched-capacitors results in a significant contribution to the output noise of SC filters. The noise of the MOST switch in the "off" state is bandlimited below a fraction of 1 Hz by the lowpass filtering action of the very high "off" resistance, and so is negligible.

The first noise component of the operational amplifier is its broadband thermal noise. This noise has a white spectral density similar to the thermal noise of MOST switches, but with a smaller equivalent noise bandwidth (B_{eq}), depending on the unity-gain frequency of the operational amplifier. Since the unity-gain frequency of the operational amplifier used in SC filters is usually

much bigger than the sampling rate (for settling time consideration), the aliased noise of operational amplifiers could be the major contributor to the output noise.

The second noise component of the operational amplifier is its flicker or 1/f noise. The magnitude of this low frequency noise component is dependent on the process used, the design of the operational amplifier used, and on the area of the input transistors in the operational amplifier. This noise could be represented by the following power spectral density[201]:

$$S_{1/f} = \frac{A_o}{f} + \rho A_o \qquad (5.17)$$

where A_o is the dc gain of the operational amplifier, it also includes the process dependence; f is the frequency of interest (usually in the passband of the SC filter); and ρ is a factor which depends on sampling frequency and is defined[102] as: $\rho = \sum_{i=1}^{N} [(if_s - f)^{-1} + (if_s + f)^{-1}]$. Therefore, using a high clock frequency decreases the second term in Eqn (5.17), so that it may be ignored compared to the first term which is unsampled noise.

In conclusion, the relative significance of the noise elements in the SC filters depends on their noise bandwidth and the topology of the SC filter[172,201]. Results for practical noise measurements are given in section 6.8.

CHAPTER 6: IMPLEMENTATION AND EXPERIMENTAL RESULTS OF THE PROTOTYPE INTEGRATED SWITCHED-CAPACITOR LOWPASS LADDER FILTER

6.1 Introduction

The SC lowpass ladder filter described in Chapter 4 was designed in integrated form using integrated circuit (IC) design facilities available in the University of Edinburgh. Design aspects will be described in section 6.2. The above SC integrated filter was then fabricated using a 5 μm, 15 V polysilicon-gate NMOS process (Appendix C) at Plessey Research (Caswell) Limited, and included in a large chip containing a number of different filter sections. Individual samples of the SC ladder filter designed in this research were assembled in 40-pin dual-in-line packages and then tested. The simplicity of the SC filter, careful design and fabrication resulted in a high yield of integrated circuits. Out of fity packaged chips, forty-five SC filters were working, which shows a yield of 90 per cent.

6.2 Implementation of the Experiemental Integrated Filter

The prototype SC lowpass ladder circuit was designed using the so-called GAELIC suite of computer programmes on the Edinburgh DEC System 10[(203)]. This integrated circuit design aid was originally developed at Edinburgh University and was then taken over by Compeda Limited, who have continued its development and now market GAELIC to other companies who design integrated circuits.

The versions of GAELIC available at the time of this circuit design were "original" GAELIC and Revision 10, which were rather inefficient in their use of computer time compared to the Revision 12 now available. However, the original version of GAELIC was very

usable and it is recognised that without it, this integrated circuit design would not have been possible.

The complete integrated circuit layout for the prototype SC lowpass ladder filter, which was a part of a large chip[84], is shown in Fig. 6.1. This integrated circuit comprised three SC integrators as shown in Fig. 4.5, with the capacitor ratios calculated in section 4.5 (Eqns (4.48) to (4.51). The smallest capacitor values viz: $C_{A1} = C_{C1} = C_{A2} = C_{A3} = C_{C3}$, were 7.92 pF (0.022 mm^2). These rather large capacitors were chosen to reduce the effects of capacitor mismatch and stray-capacitances described in sections 5.3.1 and 5.3.3 respectively. Using the stray-insensitive circuits[66,169], it is possible to reduce the size of the smallest capacitors to less than 1pF. Also to reduce the effect of oxide gradient mentioned in section 5.3.1, the capacitors associated with each integrator were laid out as close as possible.

The MOS operational amplifier employed in the prototype SC lowpass ladder filter was designed by Dr Peter B Denyer, who at that time worked with Denyer Walmsley Microelectronics Limited. Details of operation and performance characteristics of this operational amplifier, which was primarily designed for an SC wave digital filter, are reported elsewhere[193]. However, some of the target specifications for the above mentioned operational amplifier are given in Appendix D, while its measured parameters are reported in section 6.4. The micro-photograph of the SC circuit in integrated form is shown in Fig. 6.2.

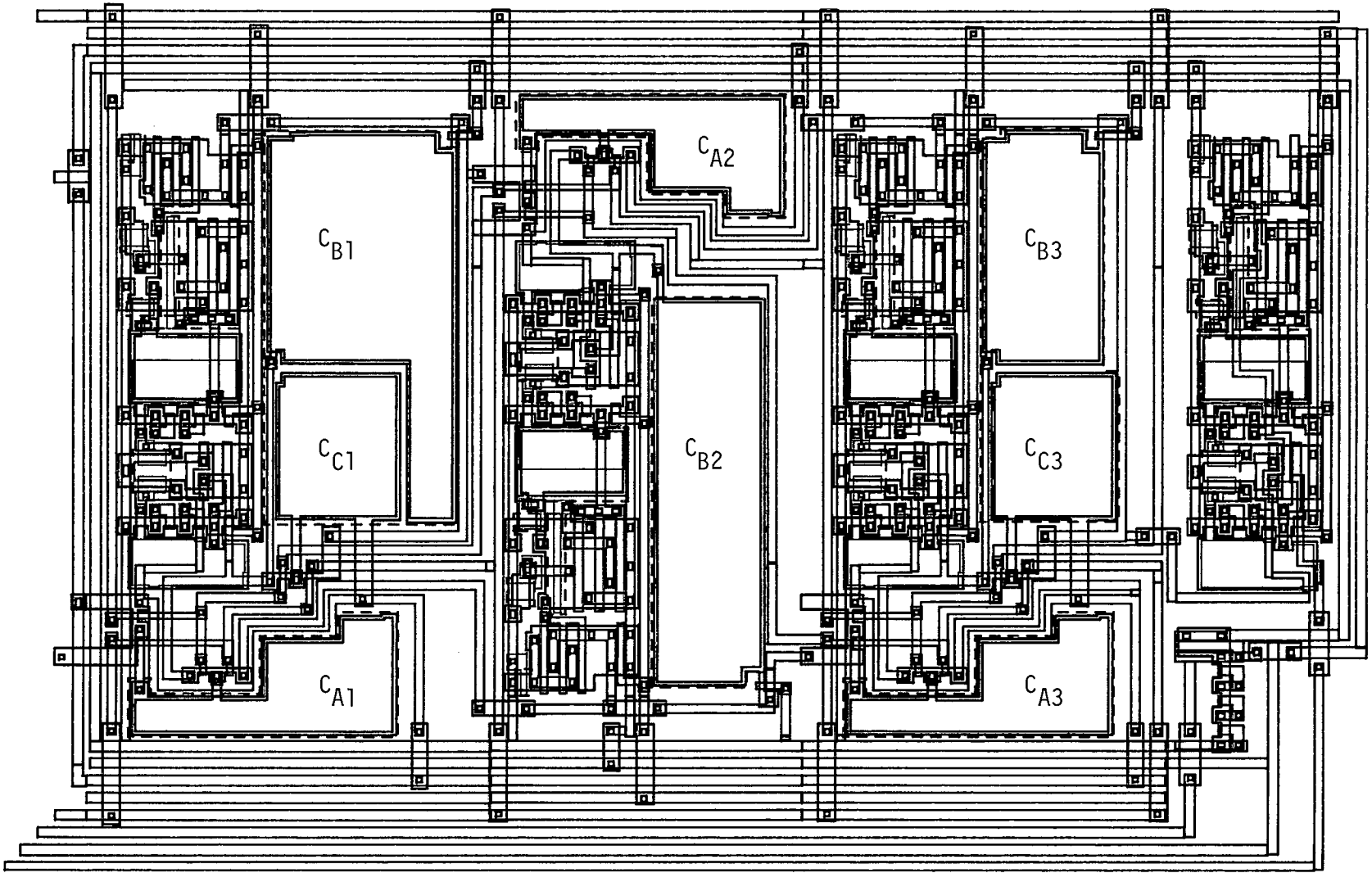


FIG.6.1: Integrated circuit layout of the experimental switched-capacitor filter shown in Fig.4.5.

Colour coding: Red = diffusion layer; blue = polysilicon one layer; black = aluminium tracks and contact holes; broken lines = depletion area. Chip size = 1000 x 1500 μm.

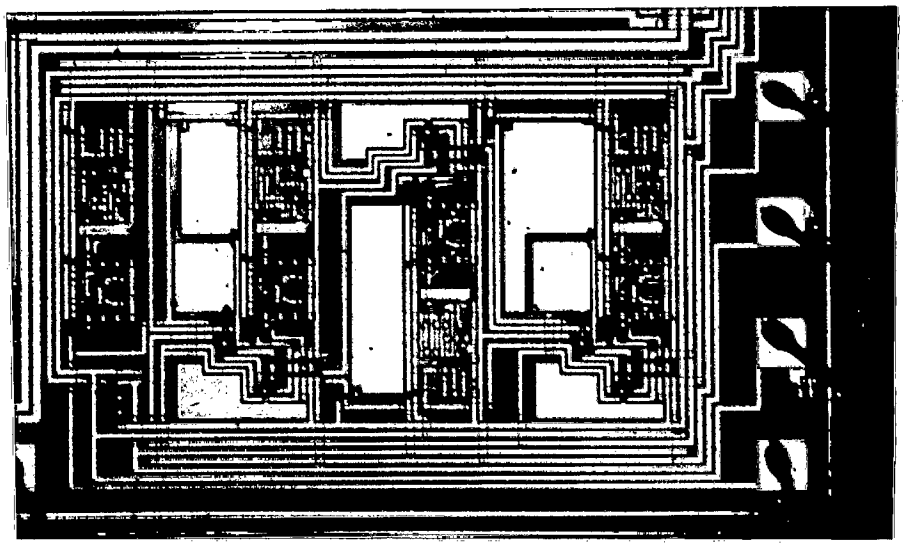


FIG.6.2: Microphotograph of the integrated circuit shown in Fig.6.1.

6.3 The Test Board

A test board was built to examine the samples of the prototype integrated SC filter. It was designed to be self-contained and provided the power supplies, reference voltage and other requirements of the integrated filter.

The main active element of the SC filter was its operational amplifier. The integrated operational amplifiers, in the prototype circuit, were designed to be supplied by zero and fifteen volts. Since the output voltage swing of the integrated operational amplifier was between 3.5 and 8.5 volts, the reference voltage which could act as the "zero" for the SC filter signals had to be selected from midway between 3.5 and 8.5 volts. The filter therefore required a voltage of about 6 volts to act as a level about which all signal voltages in the filter could be referenced. This reference voltage was named "analogue zero".

Fully smoothed and stabilised power supplies of + 15 volts and -5 volts were available on the test board. Also an adjustable external bias voltage generator was provided to override the on-chip bias voltage generator in the case of malfunction.

Finally, no anti-aliasing or output smoothing filter was used, to eliminate their predicted effects on the frequency response of the SC prototype filter. These additional filters are always included, when an SC filter is used in telecommunications applications.

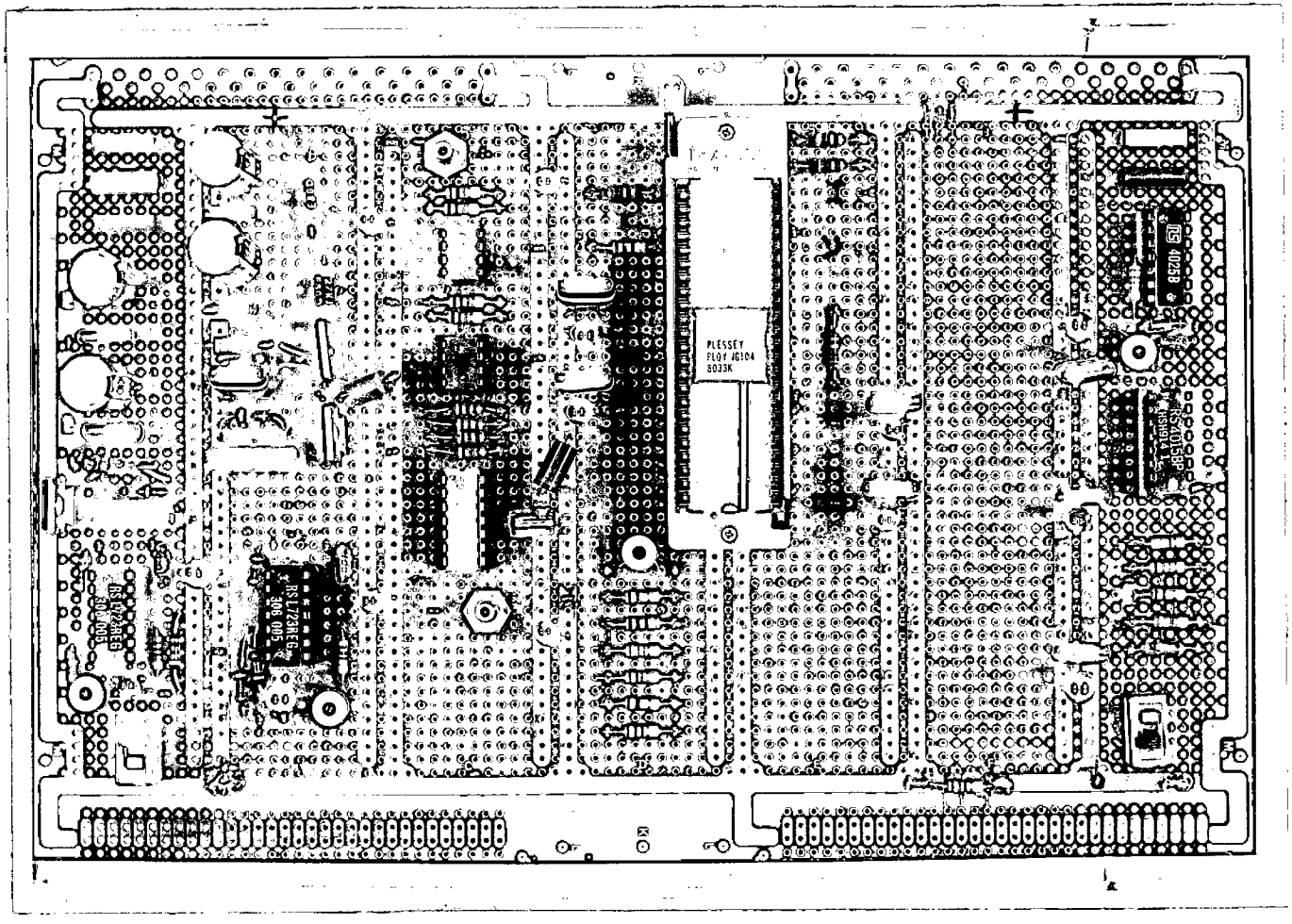


FIG.6.3: The test board for the prototype integrated switched-capacitor ladder filter.

A photograph of the test board is shown in Fig. 6.3, which was used to obtain all the results given in the next sections.

6.4 Open-Loop Gain, Unity-Gain Bandwidth, and Power Consumption of the Experimental NMOS Operational Amplifiers

The open-loop gain of the integrated operational amplifier was measured using the established methods[204,205]. The measured d.c. gain, at room temperature, was about 1500.

The unity-gain bandwidth of the operational amplifiers was measured using a spectrum analyser. For this measurement, the integrated operational amplifier was connected in a simple inverting configuration with an arbitrary closed-loop voltage gain of 20 dB. The result is shown in Fig. 6.4. In this figure, the upper trace is the closed-loop frequency response of a wideband JFET operational amplifier (LF 356), for comparison. The horizontal line is the unity-gain reference line, i.e. when the tracking generator output of the spectrum analyser is directly connected to its input. The unity-gain bandwidth of the operational amplifier is the frequency at which its frequency response intersects the unity-gain line. This procedure gave the unity-gain bandwidths of the integrated operational amplifiers to be about 0.8 MHz. However, the actual unity-gain bandwidths of the experimental operational amplifiers are expected to be higher than the measured value, because the combined effects of the large feedback resistance and stray capacitances reduce the actual closed loop response[204].

Finally, the static power consumption of the integrated operational amplifiers was measured to be 6 mW.

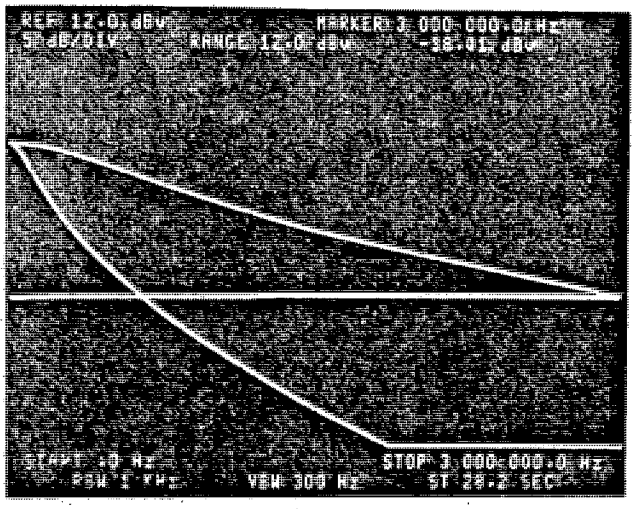


FIG.6.4: Measurement of the unity-gain bandwidths of the operational amplifiers using spectrum analyser.

Upper trace: Frequency response of the LF 356, JFET operational amplifier.

Lower trace: Frequency response of the experimental NMOS operational amplifier.

Horizontal line: Unity-gain line of the spectrum analyser.

6.5 Estimation of Parasitic Capacitances in the Experimental Switched-Capacitor Lowpass Ladder Filter

The SC lowpass ladder filter realised in integrated form, was basically formed by the interconnection of two different integrators, namely, lossless and lossy integrators. These integrators were analysed in Chapter 4, without including parasitic capacitances. Fig. 6.5 shows the above mentioned switched-capacitor lossy integrator along with all possible stray capacitances associated with both plates of MOS capacitors. Since the lossy integrator shown in Fig. 6.5 includes all stray capacitances present in the lossless integrator, the same arguments also apply to the lossless integrator. In the following, the effective stray capacitances in the SC integrators will be identified, their values will be estimated, and their effects on SC filter frequency response will be simulated using the SCNAP programme.

Figure 6.5 shows the following stray capacitances associated with capacitor C_A:

Stray Capacitance	Cause
C_{pA1}	diffusion area and perimeter of MOSFET switches connected to the top plate of capacitor C_A.
C_{pA2}	top plate inter-connection of capacitor C_A to the integrated circuit.

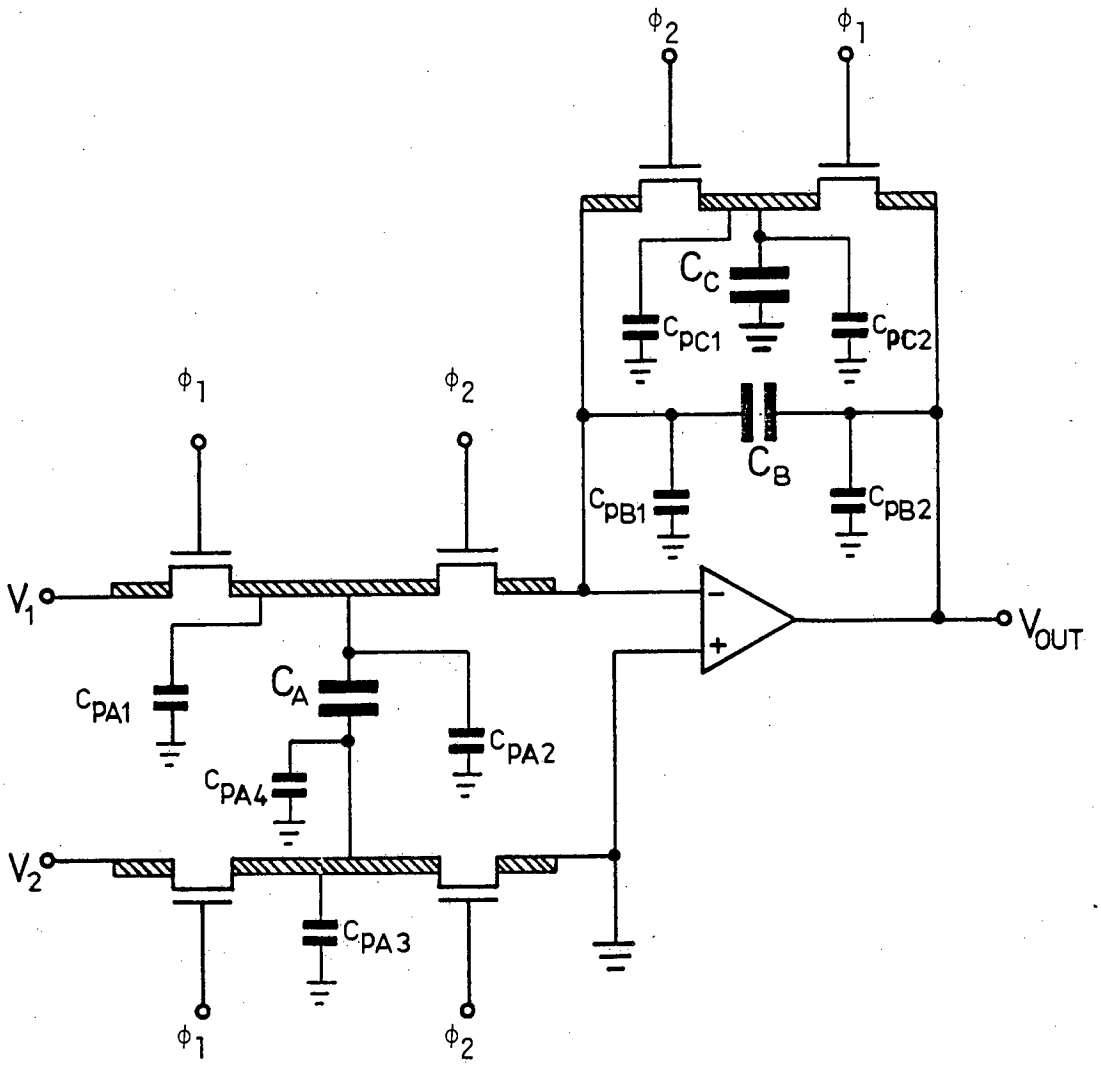


FIG.6.5: Parasitic capacitances associated with a switched-capacitor, lossy differential integrator used in the experimental integrated filter.

Stray Capacitance	Cause
C_{pA3}	diffusion area and perimeter of MOSFET switches connected to the bottom plate of capacitor C_A.
C_{pA4}	diffusion area and perimeter of bottom plate of capacitor C_A.

Since the bottom plate of capacitor C_A is either connected to voltage source (V_2 in Fig. 6.5) or to ground, the stray capacitances C_{pA3} and C_{pA4} have no effect on the integrator output. However, the stray capacitances C_{pA1} and C_{pA2} charge to voltage V_1, during the ϕ_1 phase, and their total charge will be transferred to feedback capacitor C_B. Hence the integrator output will be affected.

Stray capacitances associated with feedback capacitor C_B are as follows:

Stray Capacitance	Cause
C_{pB1}	top plate inter-connection of capacitor C_B to the integrated circuit.
C_{pB2}	diffusion area and perimeter of the bottom plate of capacitor C_B.

Assuming a high gain (> 1000) operational amplifier, neither of the stray capacitances C_{pB1} or C_{pB2} will affect the circuit performance,

because the latter is connected to a voltage source (operational amplifier output), and the former is always at virtual ground.

Stray capacitances associated with capacitor C_C are:

Stray Capacitance	Cause
C_{pC1}	diffusion area and perimeter of MOSFET switches connected to the top plate of capacitor C_C.
C_{pC2}	top plate inter-connection of capacitor C_C to the integrated circuit.

The above stray capacitances are the only significant ones associated with capacitor C_C as the bottom plate of this capacitor is already connected to ground. Note that the stray capacitances C_{pC1} and C_{pC2} have the same order of magnitude as stray capacitances C_{pA1} and C_{pA2} (see below).

From the above study it can be concluded that the integrators used in the SC lowpass ladder filter shown in Fig. 4.5, are only sensitive to the top plate stray capacitances associated with MOS capacitors C_A and C_C. These stray capacitances could be estimated using Appendix C and Fig. 6.6, as follows:

(a) Stray capacitances due to MOST switches (C_{pA1} or C_{pC1}) assuming an operating voltage of 8 volts:

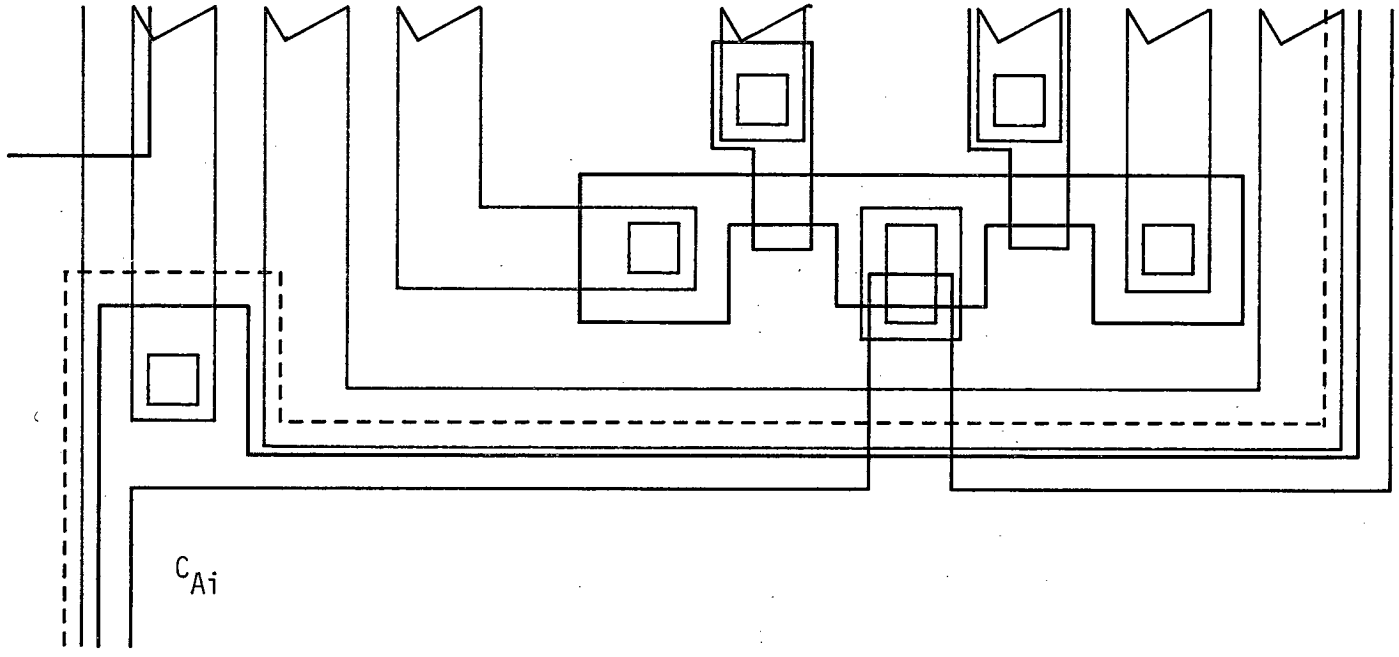


FIG.6.6: Magnified integrated circuit layout of a part of the experimental switched-capacitor filter shown in Fig.6.1, to facilitate the estimation of the parasitic capacitances associated with the top plate of the MOS capacitors as described in section 6.5.

N.B. Colour coding is as defined in Fig.6.1.

$$\text{diffusion area term} = 324\ \mu m^2 \times \frac{0.7}{(V + 0.6)^{\frac{1}{2}}} \times 10^{-4}\ pF$$

$$= 8\ fF$$

$$\text{diffusion perimeter term} = 80\ \mu m^2 \times \frac{8}{(V + 0.6)^{\frac{1}{3}}} \times 10^{-4}\ pF$$

$$= 32\ fF$$

(b) Stray capacitances due to the top plate inter-connections (C_{pA2} or C_{pC2}):

P_1 to field oxide area = $180\ \mu m^2 \times 3.6 \times 10^{-5}$ pF = 7 fF

Aluminium to P_1 = $70\ \mu m^2 \times 3.3 \times 10^{-5}$ pF = 2 fF

Aluminium to substrate = $6\ \mu m^2 \times 1.8 \times 10^{-5}$ pF = 0.1 fF

The total stray capacitances estimated in parts (a) and (b) is about 50 fF which should be added to the capacitor C_A and C_C in all integrators of SC lowpass ladder filters shown in Fig. 4.5. The computer simulated effects of the stray capacitors, on the frequency response of the integrated SC filter, are shown in Figs. 6.7 and 6.8. As it can be observed, the significant effect of stray capacitances in the frequency response of SC lowpass ladder filters is to decrease the gain in the passband.

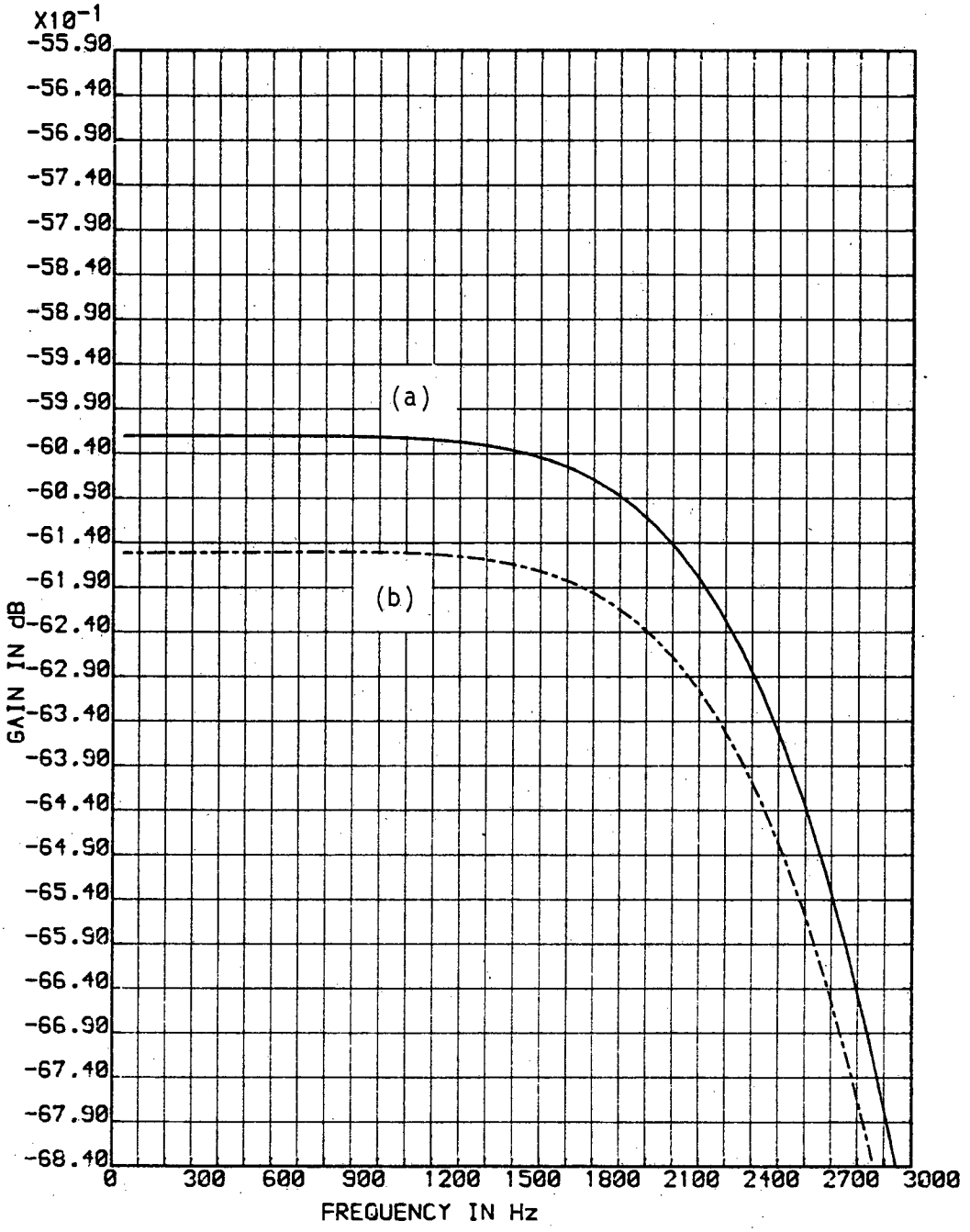


FIG.6.7: Simulated passband responses of the switched-capacitor filter shown in Fig.4.5, without parasitic capacitances (a), and with 0.06 pF parasitic capacitances (b) added to the capacitors C_A and C_C as described in section 6.5.

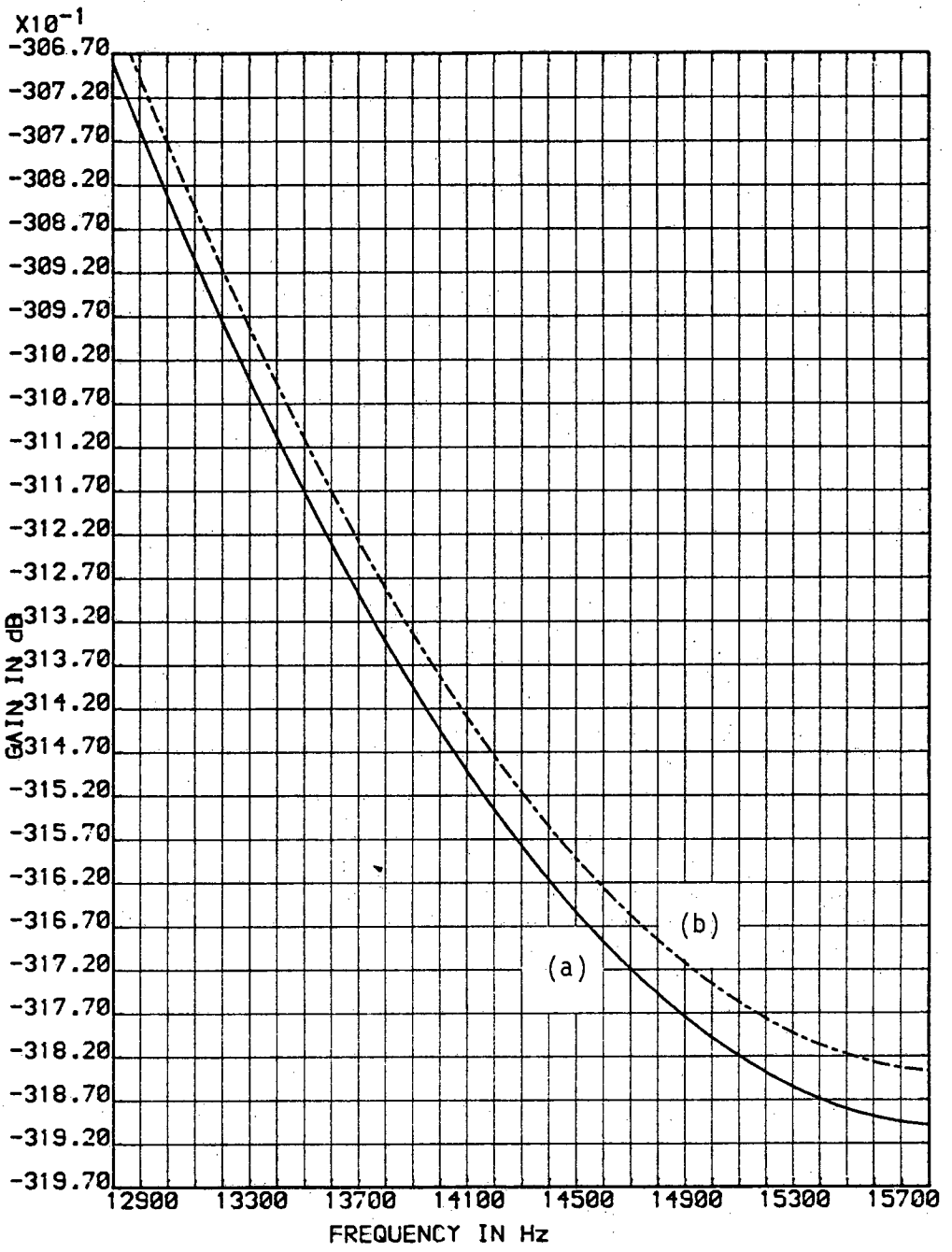


FIG.6.8: Simulated effect of the parasitic capacitances on the attenuation band of the switched-capacitor filter shown in Fig.4.5. Curves (a) and (b) have been defined in Fig.6.7.

6.6 Comparison between the Simulated and Measured Frequency Response of the Prototype Integrated SC Lowpass Ladder Filter

The frequency response of the integrated SC filter was measured using an HP 3585A Spectrum Analyser. Figs. 6.9 and 6.10 show the comparison between the measured response, and the simulated response using the SCNAP programme. In the simulated response, the effects of finite gain and bandwidth of the operational amplifiers, as well as the stray capacitances, have been considered. These effects have been evaluated in sections 5.4.1 and 6.5 respectively. It should also be mentioned that the (sin x)/x effect has been extracted from the measured response. In a typical application like a "PCM Voice Codec System", the (sin x)/x effect is automatically extracted by the receive filter.

6.7 Effect of High Clock Frequencies on the Frequency Response of the Prototype Integrated Lowpass Ladder Filter

To study the effect of high clock frequencies on the frequency response of the prototype integrated SC lowpass ladder filter, the clock frequency was increased to 550 kHz (about 17 times). The results of this experiment are shown in Figs. 6.11(a) and (b). These figures shown the spectrum analyser pictures from the passbands and also from the whole frequency responses up to Nyquist frequency (fc/2). The upper traces in both pictures are the frequency response of the SC filter with a clock frequency of 32 kHz. The lower traces belong to the same filter when a clock frequency of 550 kHz was used. In the latter case, the passband of the SC filter was extended to 550/8.25 = 66.66 kHz. Note that two different frequency ranges were used for the spectrum analyser, to make the comparison possible.

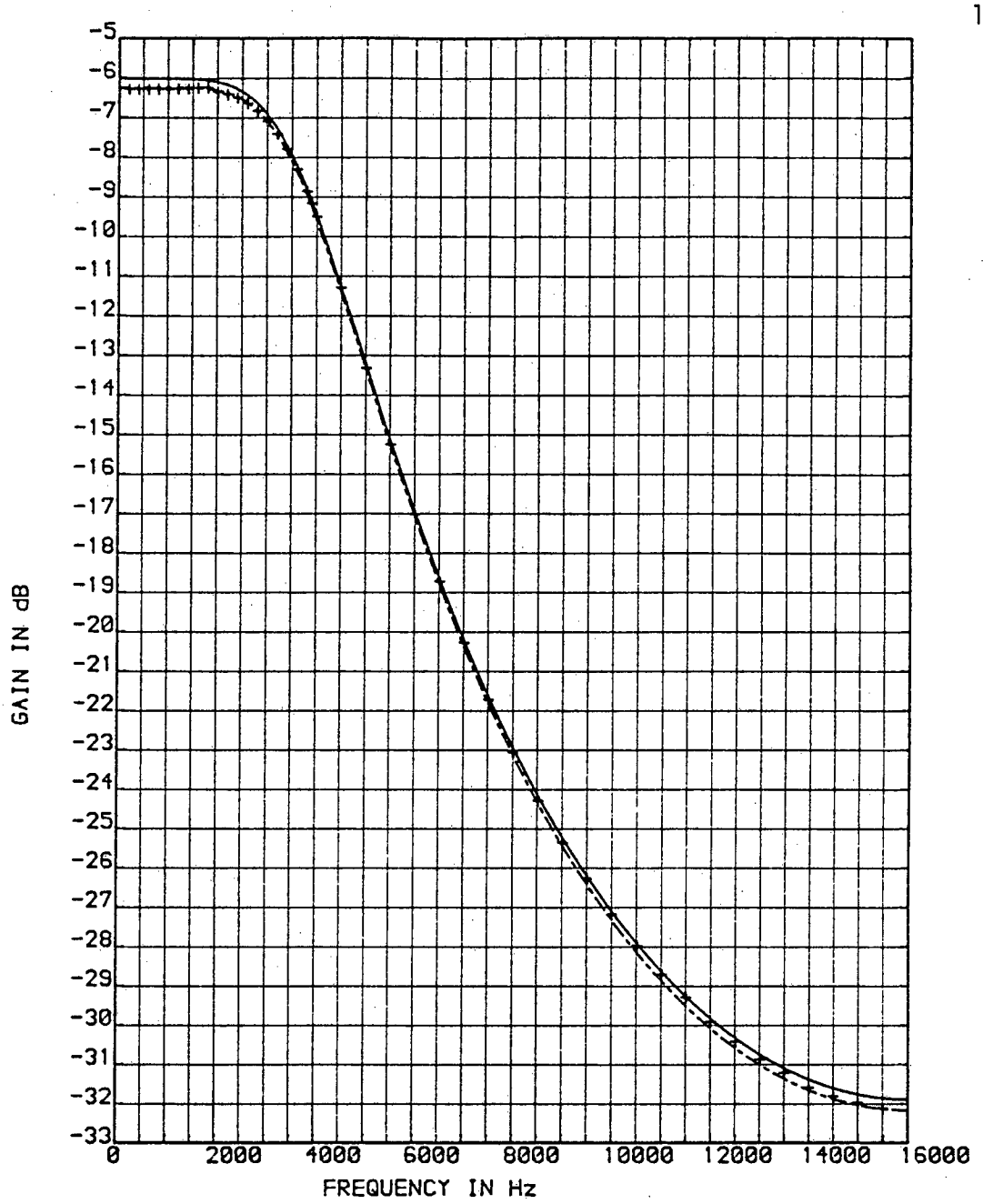


FIG.6.9: Comparison between the simulated and the measured frequency responses of the integrated switched-capacitor lowpass ladder filter.

——— Simulated response with ideal operational amplifiers and without parasitic capacitances.

—·—·— Simulated response with non-ideal operational amplifiers (gain = 1500; gain-bandwidth product = 2 MHz) and with parasitic capacitances added to the capacitors C_A and C_C (section 6.5).

+++ Measured response (sinx/x roll-off removed).

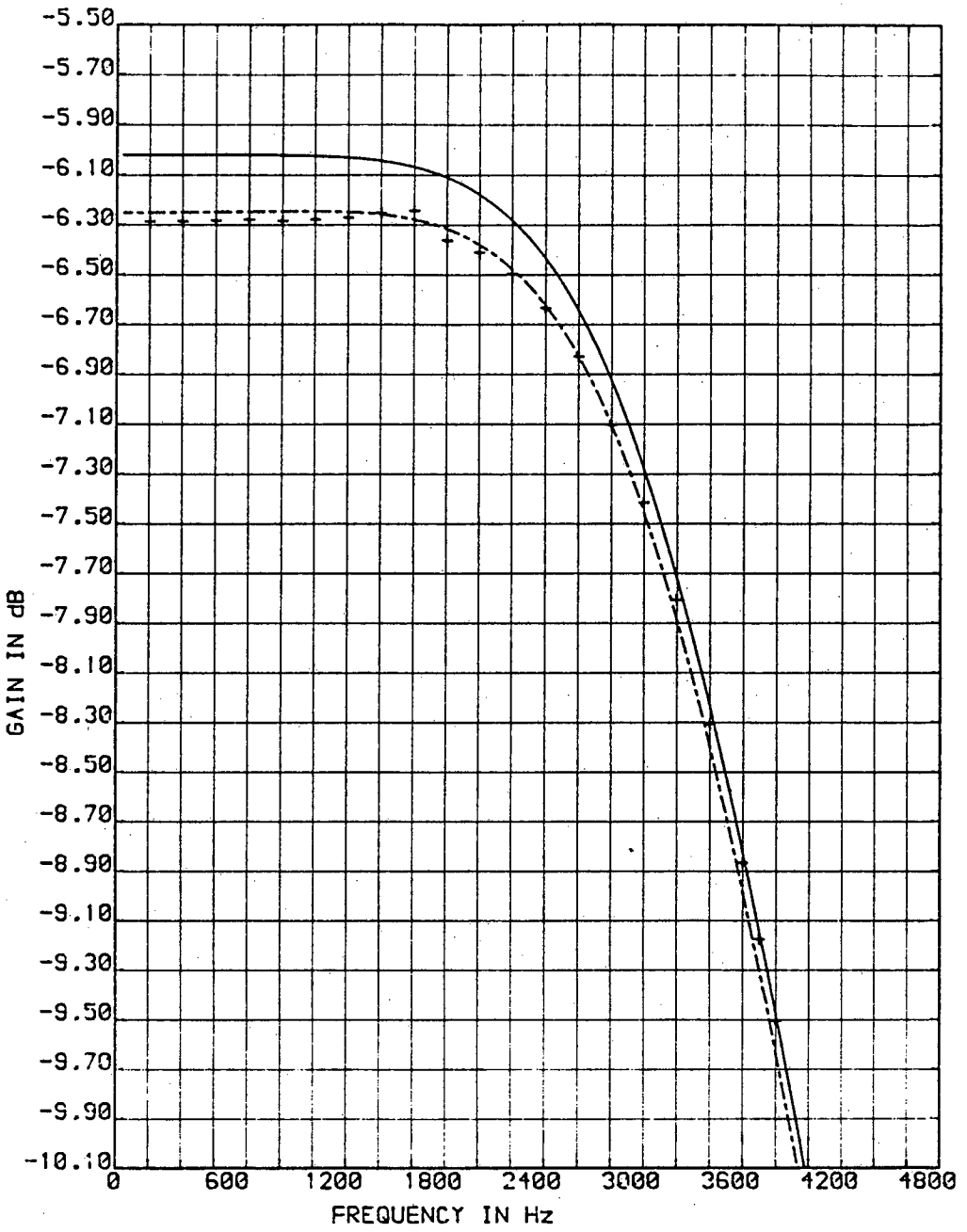


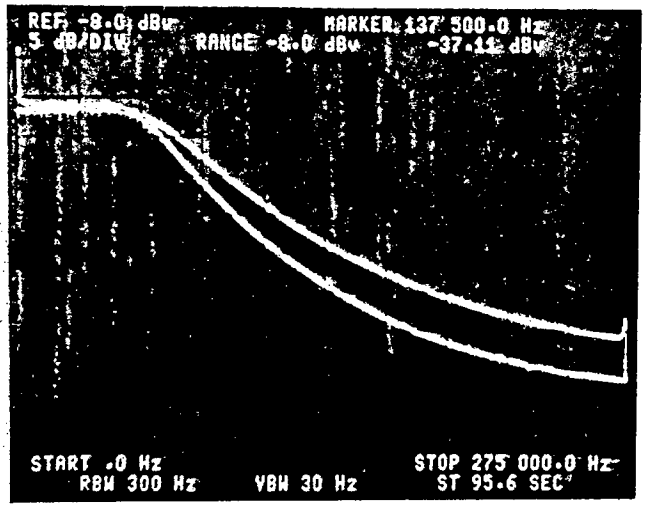
FIG.6.10: Magnified passband of Fig.6.9.

By increasing the clock frequency, the passband of the SC filter approaches the limited bandwidth of the operational amplifier. Thus the problem of limited gain-bandwidth product arises, which has been described in section 5.4.1. In fact the passband loss and frequency compression (peaking) seen in Figs. 6.11(a) and (b) have already been predicted by computer simulation given in section 5.4.1. Thus the result of this section confirms the statement given in the literature[167] that the maximum sampling frequency is limited by the settling time of the operational amplifiers employed in the SC filter.

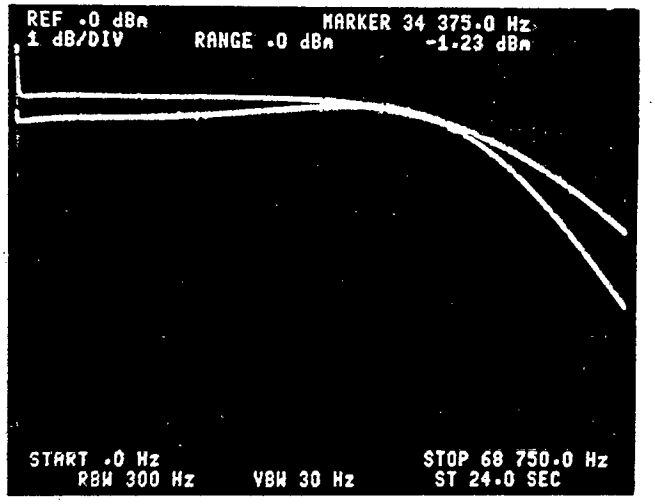
6.8 Noise Measurements

Using the test set up shown in Fig. 6.12, the spot noise measurements for the integrated operational amplifier and the prototype integrated SC lowpass ladder filter were performed.

In the case of the operational amplifier, the internally generated noise was amplified by a factor of 100, using a simple closed loop inverting configuration with grounded input[206]. This configuration is represented by a block named C.U.T. (circuit under test), in Fig. 6.12. The resulting noise was further amplified by a Brookdeal 453 low noise amplifier in order to increase the relative magnitude of the operational amplifier noise compared to the noise floor of the test channel. The noise amplified by the low noise amplifier was then filtered by a Krohn-Hite 3103 tunable bandpass filter to obtain the spot noise measurements. If the voltage transfer function of the bandpass filter is H(f), and the input noise voltage spectral density is $S_{in}(f)$, then the total mean



(a)



(b)

FIG.6.11: Effects of high clock frequency on the frequency response of the prototype integrated switched-capacitor lowpass ladder filter.

(a) Frequency responses with a clock frequency of 32 kHz (upper trace), and with a clock frequency of 550 kHz (lower trace).

(b) Magnified passband of (a).

square output noise voltage $\overline{V_{out}^2}$, is:

$$\overline{V_{out}^2} = \int_0^\infty S_{in}(f)\, H^2(f)\, df$$

$$= H_o^2\, S_{in}(f_o) \int_0^\infty \frac{H^2(f)}{H_o^2}\, df$$

$$= H_o^2\, S_{in}(f_o).\, B_{eq} \qquad (6.1)$$

where H_o is the centre frequency (f_o) voltage gain, and the passband is assumed so narrow that $S_{in}(f)$ can be approximated by $S_{in}(f_o)$. Eqn 6.1 also defines the noise equivalent bandwidth B_{eq}, which is not, in general, equal to the usual 3 dB bandwidth of the bandpass filter. However, for a bandpass filter with a relatively high order, the 3 dB bandwidth and the noise bandwidth are so close that they can be considered equal[207]. For example, the ratio of the noise bandwidth to the 3 dB bandwidth (B_{eq}/B_{3dB}), for a fourth-order bandpass filter, is 1.1, whereas the same ratio for a second-order bandpass filter is 1.2. The bandpass filter used in the noise measurement comprised a highpass filter and a lowpass filter both having fourth-order voltage transfer function (24 dB per octave roll off) and a maximum attenuation of 80 dB. Hence, this bandpass filter has a 3 dB bandwidth that can be considered to a good approximation to be the noise bandwidth.

The noise filtered by the bandpass filter was then measured by a Hewlett-Packard 3400A true r.m.s. voltmeter. In noise measurements, a true r.m.s. voltmeter is always preferred, because noise changes from uncorrelated sources add quadratically and a quadratic detector, whose output is proportional to the square of the input voltage, is desired. The frequency range of the true r.m.s. voltmeter was 10 Hz

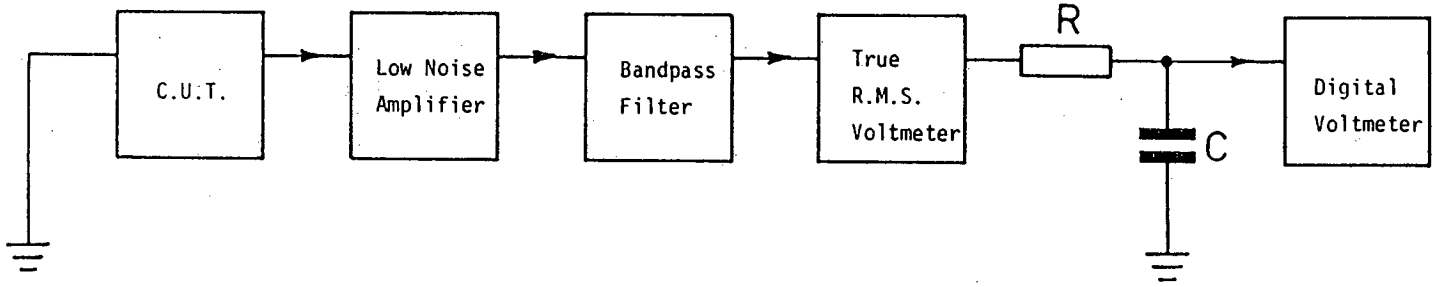


FIG.6.12: The noise measurement channel for the experimental operational amplifier and the switched-capacitor lowpass ladder filter.

to 10 MHz, with a wide dynamic range from -72 to +52 dBm (0 dBm = 1 mW into 600 Ω).

Although the r.m.s. value of noise averaged by a long time-constant approaches a fixed value, the instantaneous noise amplitude is totally random and, therefore, the reading fluctuated about the mean value. To improve the accuracy of the measurement, by averaging the noise signal over a long period of time, a d.c. output proportional to the scale reading available at the rear of the instrument, was put through a single RC time-constant lowpass filter of time constant $\tau = RC$, into a digital voltmeter. When an averaging circuit is used in conjunction with a true r.m.s. voltmeter, the probable error of a single noise reading is[207]:

$$\text{Error} = 100\ (2\ B_{eq}\ \tau)^{-\frac{1}{2}}\ \% \qquad (6.2)$$

where B_{eq} is the noise bandwidth. By employing a value of τ from 1 second to 10 seconds, this error was kept below 2%.

Using the measurement channel shown in Fig. 6.12, and described above, the low frequency spot noise and the output wideband noise of the integrated operational amplifiers were measured. The output wideband noise of a typical operational amplifier measured between 10 Hz and 16 kHz (the Nyquist rate) was 75 μV r.m.s. Thus their equivalent r.m.s. voltage was about 600 $nV/\sqrt{Hz}$. Similarly, the output wideband noise of the prototype integrated SC lowpass ladder filter within the same bandwidth was obtained as 2.3 mV r.m.s. Thus its output noise voltage per unit bandwidth is 18 $\mu V/\sqrt{Hz}$. Input

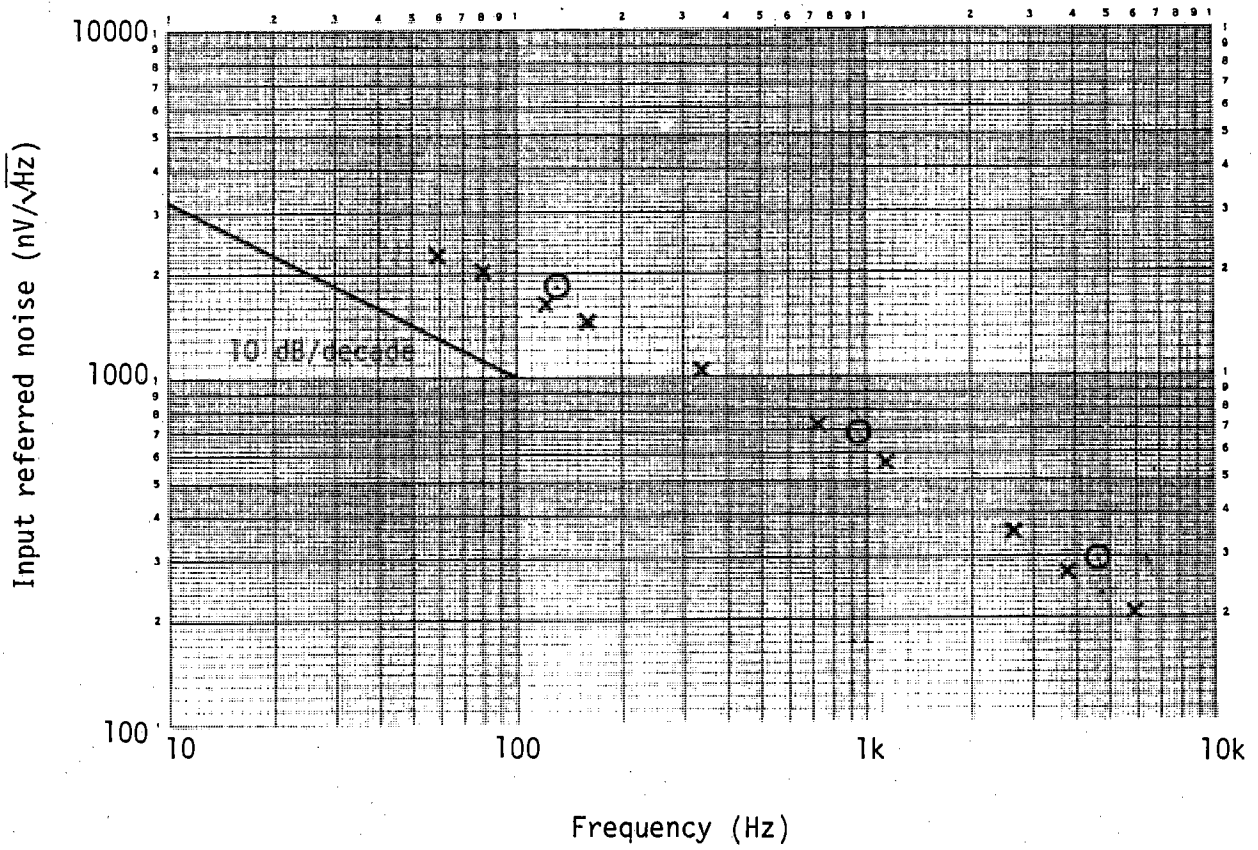


FIG.6.13: Comparison of spot noise measurements for the experimental operational amplifier using the measurement channel shown in Fig.6.12(xxx), and using HP-3585A spectrum analyser (ooo).

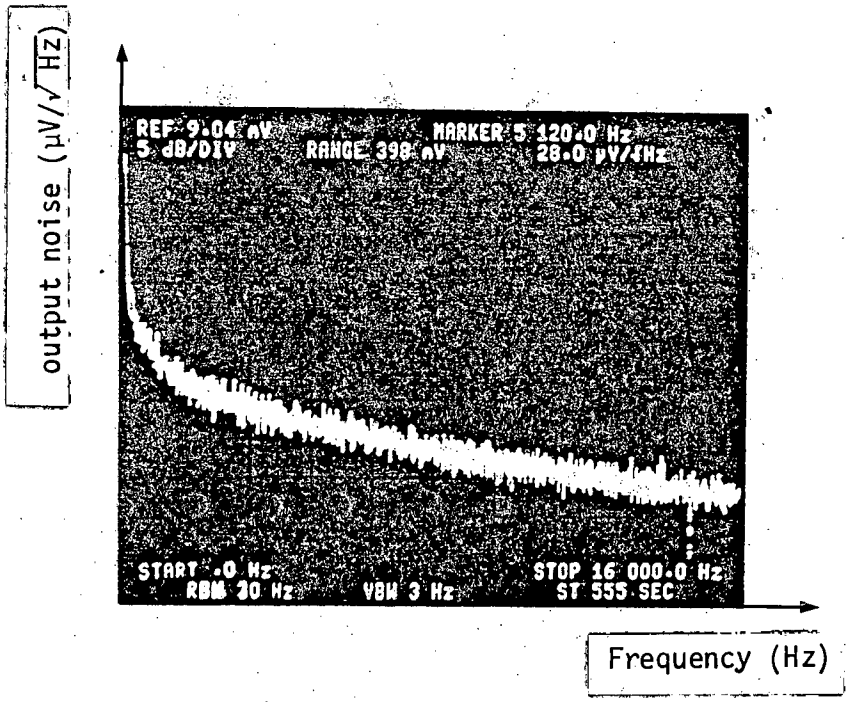


FIG.6.14: Low frequency (1/f) noise spectrum of the experimental operational amplifier.

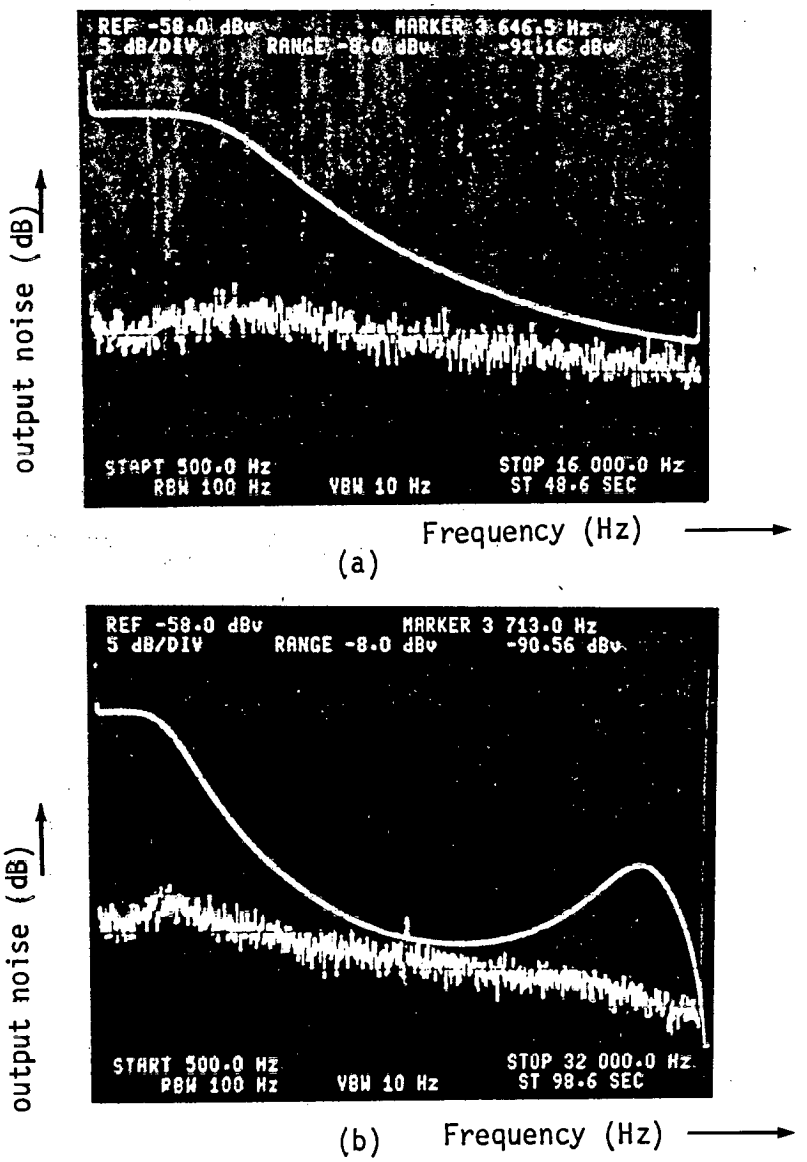


FIG.6.15: Noise spectrum of the prototype integrated switched-capacitor lowpass ladder filter up to the Nyquist frequency (a), and up to the clock frequency (b).

N.B. Frequency response of the sc filter has also been shown for comparison. Noise has been amplified by 50 dB for comparison.

referred noise may be obtained by dividing output noise by the gain of the filter (1/2).

The spot noise measurement of the 1/f spectrum of the integrated operational amplifier up to 10 kHz was performed. The results are shown in Fig. 6.13. In the same figure the results obtained from the spot noise measurement using the automatic facilities provided in HP 3583A spectrum analyser are also included. The closeness of the two sets of measurements confirms the validity of the noise measurements using the test set up shown in Fig. 6.12.

A spectrum analyser picture of 1/f noise of the integrated operational amplifier is shown in Fig. 6.14. The noise spectrum of the prototype integrated SC lowpass ladder filter, along with its frequency response, is shown in Fig. 6.15.

6.9 Harmonic Distortion Measurement

The total harmonic distortion produced by the SC ladder filter was measured using the spectrum analyser. A typical result is shown in Fig. 6.16. As can be observed from this figure, the maximum output signal at less than one per cent (40 dB) harmonic distortion is 2 volts peak-to-peak (P-P), which is rather low. The main reasons for increased harmonic distortion are: the type of MOS capacitor used (section 5.3), the stray capacitances associated with MOST switches (section 5.2.3), and the small output swing (3.5 - 8.5 volts) of the integrated operational amplifiers.

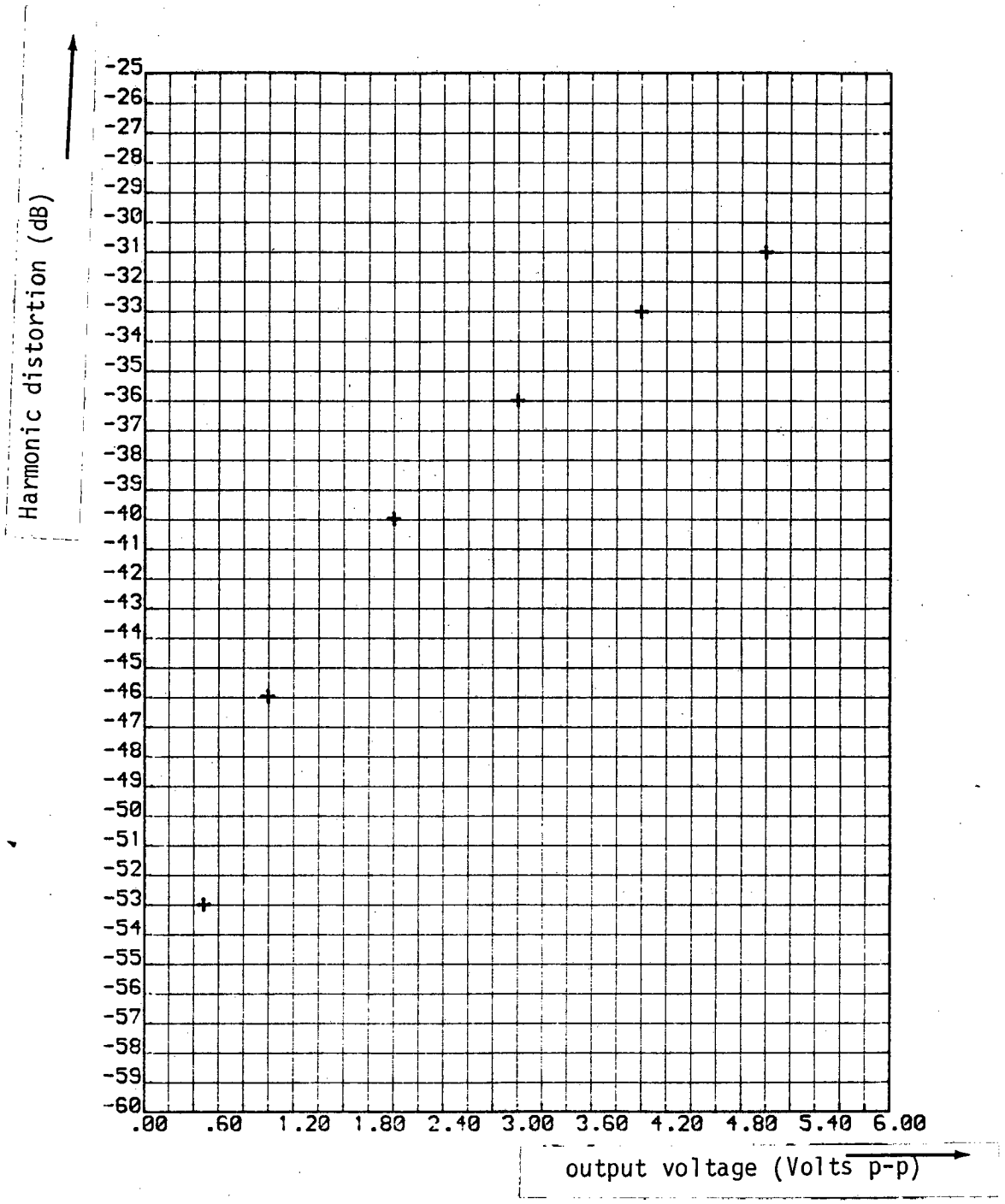


FIG.6.16: Measured harmonic distortion of the prototype integrated switched-capacitor lowpass ladder filter.

6.10 Dynamic Range

There are many different definitions of dynamic range in the literature[208,209], and so a choice has to be made of the definition to be used in this thesis. The dynamic range will be defined to be the ratio in dB of the maximum peak-to-peak (P-P) output signal of the filter (at one per cent harmonic distortion), to the output referred r.m.s. noise voltage (V_{no}) from the filter when its input is grounded, i.e.

$$DR = 20 \log_{10} \left[\frac{(V_{o.max})\ P\text{-}P}{V_{no}} \right] \qquad (6.3)$$

using the experimental results given in sections 6.8 and 6.9, the dynamic range of the integrated SC ladder filter was obtained as 95 dB at 1 kHz.

CHAPTER 7: CONCLUSIONS

The purpose of this thesis was to investigate the design of some selected SC filters for MOS implementation. As a result, three different SC biquad resonators, an SC tracking filter, and an SC lowpass ladder filter were designed and implemented, for which the experimental results were presented in Chapters 3 and 6.

In the first part of Chapter 3, a single-operational amplifier and a multiple-operational amplifier SC biquad resonator were designed and implemented using discrete components. Also a fourth-order SC bandpass filter was designed and constructed using two cascaded multiple-operational amplifier biquad resonators. The single-operational amplifier SC biquad resonator had the advantage of being programmable both by clock frequency and by a capacitor ratio. Change of clock frequency would result in the change of centre frequency, leaving the quality factor (Q) and gain (G) of the filter unchanged, while changing the particular capacitor ratio would result in the change of centre frequency, providing a constant gain and bandwidth (B) response. Both properties have applications in tracking filters[21]. Unfortunately, the single-operational amplifier SC biquad resonator is not as useful as its active-RC counterpart, because the SC circuit is sensitive to parasitic capacitances and moreover, for higher Q factors, unacceptable capacitor ratios are required, e.g. a capacitor ratio of 10,000 for a Q of 50.

Although by applying compensation techniques or by the method presented in section 3.3, the sensitivity of this single-operational amplifier SC biquad resonator filter to parasitic capacitances may

be greatly reduced, the problem of huge capacitor ratios still remains. Therefore, if the parasitic compensation techniques are applied, the integrated form of the single-operational amplifier SC filter described in section 3.2, may find some applications in low Q filtering.

Practical problems associated with single-operational amplifier SC biquad resonators, directed the investigation to other second-order SC filters, derived from useful active-RC prototypes. The well-known state-variable biquad filter was then examined. Advantages of this filter from an integrated circuit point of view are the absence of floating nodes, and the possibility of realising high-Q filters with acceptable capacitor ratios. During this investigation, a systematic approach to the design of stray-insensitive SC biquad filters was suggested. This approach, although not completely independent of previous investigators is considered as a generalised approach to the direct design of SC biquad filters from active-RC prototypes. Stray-insensitive designs facilitate the realisation of high-Q filters because, for large capacitor ratios, the smaller capacitors may be chosen as small as 0.1pF, to keep the overall size of the chip as economical as possible. For example, in the state-variable SC biquad resonator, a maximum ratio of 100 is required to obtain a Q of 50, resulting in a capacitor value of 10 pF for larger capacitor, which is quite acceptable.

A disadvantage of state-variable SC biquad filters described in section 5.3 is that only realisation of programmable, constant Q (and not constant bandwidth) filters was possible.

A fourth-order resonator was designed and breadboarded using two cascaded, second-order, state-variable SC resonators to demonstrate the

feasibility of higher order SC filters using the cascaded approach.

As a typical application of the SC biquad resonator described in the first part of Chapter 3, an SC tracking filter was designed and implemented using phase-locked loop and frequency multiplication techniques. This tracking filter was significant in the sense that no similar work had been reported at the time that this research commenced (1980). The only problem associated with the early versions of the tracking filter was the sensitivity of the SC biquad resonator employed to the parasitic capacitances, which was improved at the later stages of this research. The realisation of this SC tracking filter was regarded as a contribution to the future realisation of fully-integrated MOS SC tracking filters.

Tracking filters are somewhat similar to phase-locked loops, but are superior to them in areas where the amplitude information of the input signal are to be retained. Natural applications include automatic equalisation and FM demodulation. Typical specifications for the bandpass filter used in the tracking filter application in this thesis, i.e. a centre frequency of 1 kHz, 3 dB bandwidth of 60 Hz and tracking bandwidth of ± 500 Hz, shows that the SC tracking filter described (in the second part of Chapter 3), is capable of being employed in practical applications[12]. The expected frequency range is from tens of Hz to tens of kHz depending on the maximum permissible clock frequency limited by the settling time of the operational amplifiers present in the filter. The bandpass filter employed in the above-mentioned SC tracking filter may be replaced by other types of filters such as lowpass, highpass and notch filters, to extend the range of applications.

As mentioned in Chapter 1, the major part of this thesis concerns the design and monolithic implementation of an SC lowpass ladder filter based on a novel exact analysis and synthesis method[17]. This exact design method is superior to the conventional design method for the following reasons:

(a) Unlike the conventional design, there is no restriction on the clock frequency (apart from that which is common to all sampled-data systems, and the limitations imposed by the practical operational amplifiers). This advantage results in a much wider passband compared to the SC lowpass ladder filters obtained from the approximate design, and extends the application of SC filters to high frequency telecommunications and video applications.

(b) The capacitor ratios are obtained optimally and at the same time lower than those obtained from the approximate design. This has a twofold advantage. Firstly, if for any reason including parasitic capacitances, large capacitor values have to be selected, then the total area occupied by the capacitors are much smaller than that obtained by the conventional design. Secondly, if for slew rate and settling time considerations of practical operational amplifiers, small capacitors have to be chosen, then the largest capacitors are much smaller in the exact design.

(c) Problem of improper terminations which is present in the conventional design of SC ladder filters no longer exists in the exact design. These terminations are accounted for, in the exact analysis given in section 4.5.1.

In Chapter 4, theoretical aspects of the exact design method were described. Step-by-step analysis and synthesis for a third-order maximally flat, all-pole, lowpass ladder filter, and finally a comparison between the exact and approximate design were also presented in this chapter. MOS implementation aspects and the experimental results for the NMOS integrated lowpass ladder filter were presented in Chapters 5 and 6. Both computer simulations and experimental results confirmed the validity of the exact design method for low clock to cut-off frequency ratios.

Experimental results as well as computer simulations indicated that the most significant parameter affecting the frequency response of the experimental SC lowpass ladder filter was parasitic capacitances associated with MOS transistor switches and capacitors.

Noise and harmonic distortion measurements were performed to obtain the dynamic range of the experimental SC ladder filter. A dynamic range of 95 dB was obtained despite the use of single polysilicon layer in MOS capacitors.

Future work in the field of SC biquad filters, should include stray-insensitive design of SC filters based on the active-RC prototypes which have proved to be useful in different branches of electronics. As

an example, a programmable high-Q bandpass filter with constant gain and bandwidth will find applications in tracking systems.

Applying sampled-data techniques for the design of individual components of a tracking filter such as phase detectors or voltage-controlled oscillators and subsequent MOS implementation, will be a significant contribution to the field of adaptive systems. Different techniques for improving the capture and tracking ranges should also be investigated.

Computer simulations as well as experimental results given in Chapter 6, revealed that in any future monolithic realisation of SC ladder filters, a parasitic insensitive circuit as well as double polysilicon capacitor structure could be employed.

Future work could focus on the exact design of high-order lowpass ladder filters with finite zeros of transmission. Trade-offs between the clock frequency, capacitor ratios, and noise in SC ladder filters is another subject which is significant from the practical point of view. Recently, the exact design of elliptic lowpass ladder filters[210] and also the exact design of maximally flat bandpass ladder filters[211] have been introduced.

Finally, it is certain that with the advent of VLSI it is inevitable that digital techniques will become dominant in integrated filter design, but for the foreseeable future, switched-capacitor filters will be used in many applications where space, power and weight are crucial.

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APPENDIX A: SCNAP PROGRAMME

SCNAP (Switched-Capacitor Network Analysis Programme) has been written and developed in the University of Hull[139-141], and was then made available to Edinburgh and other UK universities via ICF (Interactive Computing Facilities) network. This programme is run by the IBM 360/195 at Rutherford Laboratory, but both input and outputs are handled by the PRIME B at Rutherford.

The SCNAP programme is based on nodal techniques[122] and was initially designed to analyse two-phase networks in the frequency domain. In this technique the two clock phases in the SC network are designated as "even" and "odd" (see Fig. A.1(a)). Then the SC networks are analysed as time-variant sampled-data networks, which can be viewed as tandem connection four-ports in the z-domain[123], as shown in Fig. A.1(b). One pair of ports is viewed as a signal path corresponding to the even time slots, the other pair of ports as a path corresponding to the odd time slots of the periodically operated switches. However, the two paths are linked by the charge-storage properties of the capacitors.

Using the above principle and deriving the definite admittance matrices for passive and active elements in the SC network, Sewell et al[140] developed the SCNAP programme, which provided a means for the exact analysis of SC networks. The main advantages of this programme are the simplicity of the input data, and the ability to include operational amplifiers with finite gain and bandwidth. Fig. A.1(c) shows an approximate frequency response of the operational amplifier used in this programme.

Currently, two versions of the SCNAP programme are available, namely SCNAP1 and SCNAP2. The SCNAP1 programme provides analysis of SC networks with two-phase clocks, while the SCNAP2 programme is capable of analysing SC networks with multiple-phase clocks. In addition, the SCNAP2 programme is able to compute the responses of the two-phase SC networks more accurately than the SCNAP1 programme[141]. An example of SCNAP input data is shown in Fig.A.2. As can be seen, this input data can be divided into three sections: heading, network description and frequency range.

The output data provides four different transfer functions (H_{ij}) according to the following matrix equation:

$$\begin{bmatrix} V^{e}_{out}(z) \\ V^{o}_{out}(z) \end{bmatrix} = \begin{bmatrix} H_{ee}(z) & H_{eo}(z) \\ H_{oe}(z) & H_{oo}(z) \end{bmatrix} \begin{bmatrix} V^{e}_{in}(z) \\ V^{o}_{in}(z) \end{bmatrix} \qquad (A.1)$$

Usually two or three of the transfer functions H_{ij} are zero depending on when the input switches are closed and when the output signal is sampled. In addition, for each existent transfer function, the phase and frequency responses are available.

Because of the large number of nodal charge equations, and a point by point computation with $z^{-1} = e^{-j\omega T}$ (and subsequent numerical matrix inversion), the run time and storage requirement for the SCNAP programme are relatively high compared to the equivalent programmes. However, this aspect of the SCNAP programme did not cause any problem

as the majority of the SC circuits used in the present thesis were low or medium order filters.

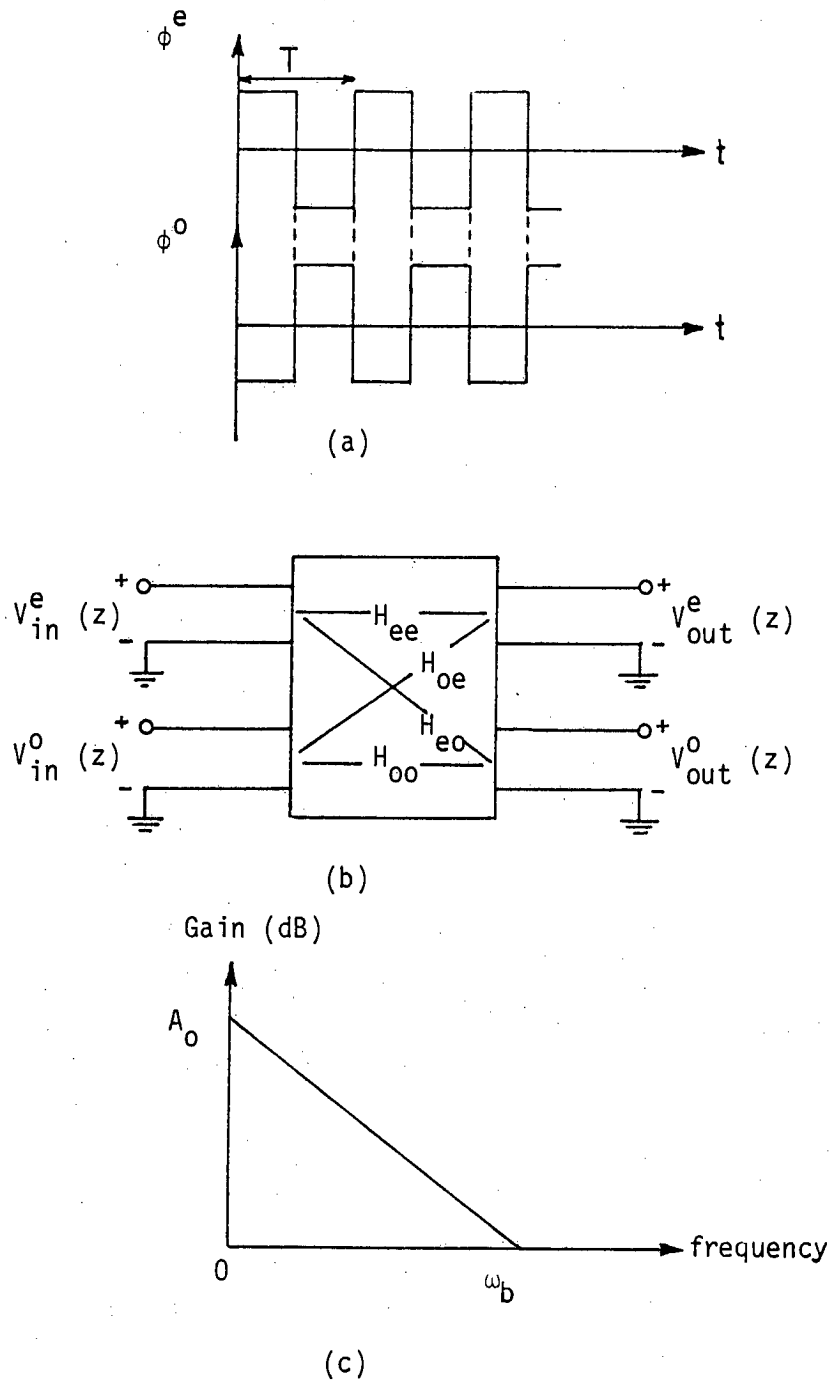
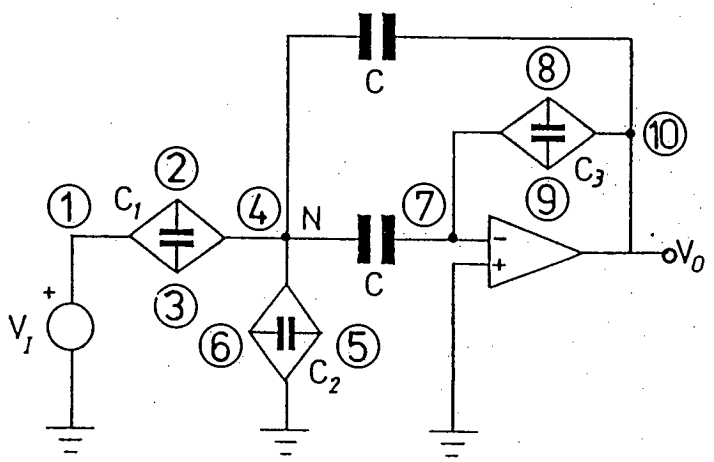


FIG.A.1: (a) Two-phase non-overlapping clocks.

(b) Switched-capacitor network equivalent system in the frequency domain.

(c) Approximate amplitude response of the operational amplifiers.




```
TR1
IGMFB
!
10  2
C  51.78P  2  3
C  1.61N  5  6
C  25.9P  8  9
C  1.0N  4  7
C  1.0N  4  10
S  1  2  1;
S  3  4  1;
S  1  3  2;
S  2  4  2;
S  4  5  1;
S  0  6  1;
S  4  6  2;
S  0  5  2;
S  7  8  1;
S  9  10  1;
S  8  10  2;
S  7  9  2;
F  8.0K
OA  356  0  7  10
1000000  0  1
END
10
1  1
1
500  1500  5
```

FIG.A.2: An example of SCNAP2 input data.

APPENDIX B: PARASITIC CAPACITANCES ASSOCIATED WITH SWITCHED-CAPACITOR BER ELEMENTS

Comparison between the simulated and measured frequency responses of the single-operational amplifier, switched-capacitor biquad resonator, shown in Fig.3.2, indicated that, despite the advantages of the switched-capacitor BER elements in deriving the switched-capacitor filters from the active-RC prototypes (c.f. section 3.2), they were practically inefficient. The main reason is their sensitivity to the parasitic capacitances shown in Fig.B.1, already described by Temes et al[20], and Nossek et al[150]. This was confirmed by computer simulation, using the SCNAP programme. The result is shown in Fig.B.2. In this figure, in addition to the simulated and measured frequency responses already shown in Fig.B.2, the frequency response of the same filter is given, which has been obtained by adding 30 per cent parasitic capacitances to both plates of all switched-capacitors ($C_{p1} = C_{p2} = 0.3C$ in Fig.B.1) and also to the floating node (N)in, Fig.3.1(b).

In conclusion, in the switched-capacitor circuits containing switched-capacitor BER elements, either the parasitic compensation methods[61], or the modified BER elements, described in section 3.3, should be adopted.

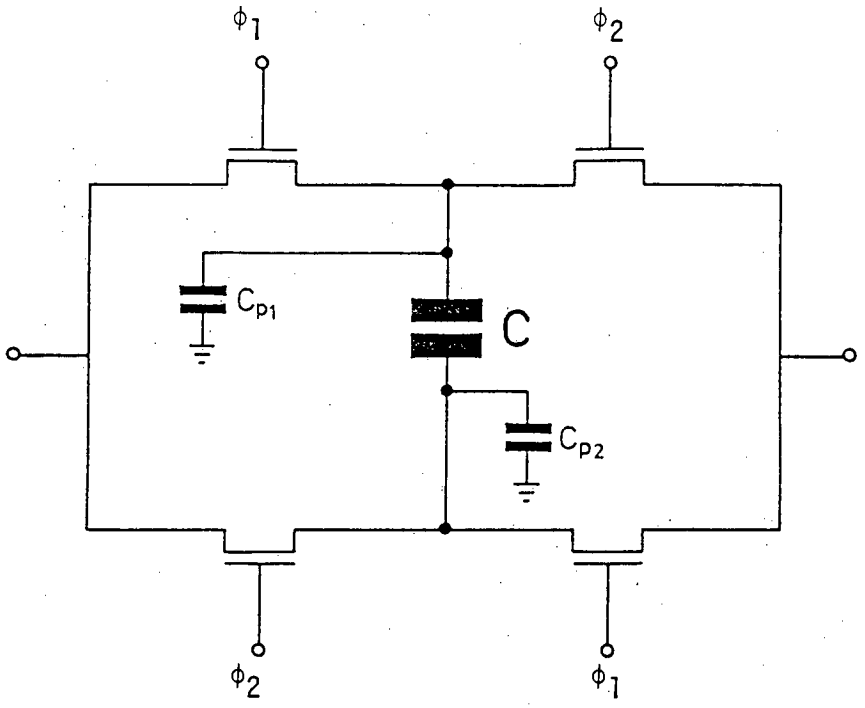


FIG.B.1: Switched-capacitor BER element and its associated parasitic capacitances.

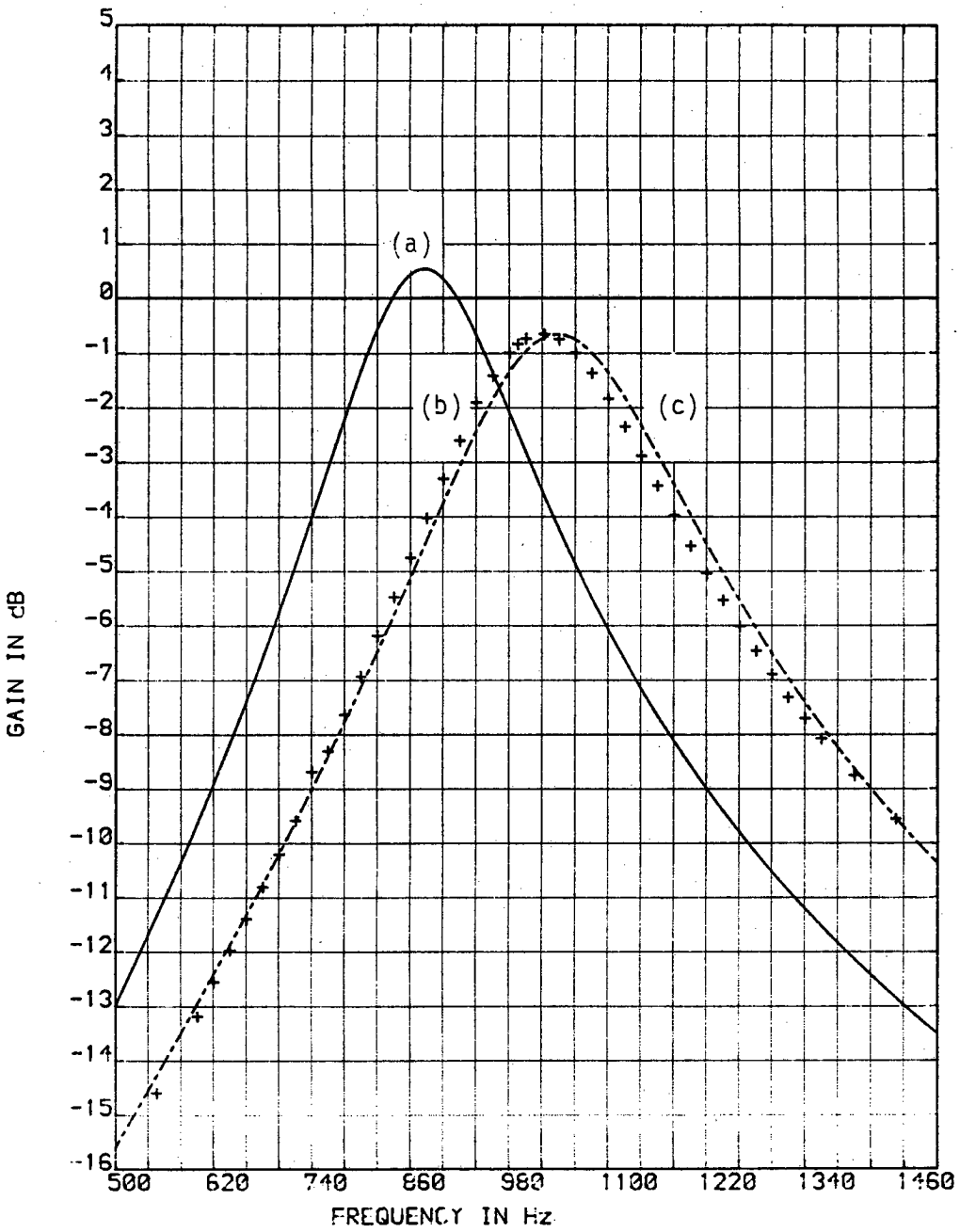


FIG.B.2: Effect of parasitic capacitances associated with the BER elements and the floating node (N) shown in Fig. 3.1(b); on the frequency response of the switched-capacitor biquad resonator.

(a) Simulated response before adding parasitic capacitances.

(b) Measured response.

(c) Simulated response after adding parasitic capacitances.

APPENDIX C: PLESSEY LAYOUT RULES

CIRCUIT IMPLEMENTATION.

The following layers are available:

Layer 1 Active Areas.

Layer 2 Depletion Areas.

Layer 4 Polysilicon Layer 1.

Layer 5 Polysilicon Layer 2.

Layer 6 Contacts.

Layer 8 Aluminium.

Layer 9 Passivation.

LAYER 1. ACTIVE AREA AA.

Active areas (e.g. MOST's, n^+ underpass) are defined by layer one. Everywhere outside the defined areas will have thick field oxide plus a self-aligning ion implant for spurious threshold control.

The active area boundary defines all components of the device (e.g. for MOST's it defines the source, gate and drain regions).

The active areas may be overlaid by polysilicon level one (layer 4) or polysilicon level two (layer 5). Any areas defined within the active area and not overlaid by polysilicon gates will become n^+.

LAYER 2. DEPLETION AREA DA.

Devices contained within both the active area and depletion area windows will have negative threshold voltages and thus will be depletion

MOST's. Devices within the active area, but not within the depletion area, will have positive threshold voltages and thus will be enhancement MOST's.

LAYER 4. POLYSILICON LEVEL 1 P1.

This may be used to implement MOST gates, capacitors (to polysilicon level two or aluminium) and for interconnections.

Overlap over n^+ areas will be approximately 1.25 microns and will be independent of alignment.

LAYER 5. POLYSILICON LEVEL 2 P2.

This may be used to implement MOST gates, capacitors (to polysilicon level one or aluminium) and for interconnections.

Overlap over n^+ areas will be approximately 1.25 microns and will be independent of alignment.

LAYER 6. CONTACTS CT.

Contact holes may be opened to n^+ diffusion or polysilicon levels one or two. Contacts to polysilicon may not be opened within the active area regions.

LAYER 8. ALUMINIUM AL.

This is a passive level for interconnections and bond pads and may not be used for active gates. The aluminium level has low capacitance and low sheet resistance and is therefore suitable for long interconnections and bus bars.

LAYER 9. PASSIVATION PA.

The completed circuit is sealed by a deposited glass for chemical passivation and scratch protection. Layer nine is also used to open windows through this glass to the bond pads.

LAYOUT RULES.

All dimensions are given in microns.

LAYER 1 AA.

Tolerance w.r.t drawn feature size	=	-1.5 to -2.5
Minimum pass-under width	=	6
Minimum separation n^+ to n^+	=	7
Minimum channel width	=	6
Minimum channel separation	=	5
Minimum separation, n^+ to unrelated gate oxide	=	5

LAYER 2 DA.

Minimum overlap around active area	=	3

LAYER 4 P1.

Tolerance w.r.t drawn feature size	=	+ or - 0.5
Minimum rail width	=	6
Minimum length MOST gates	=	6
Minimum separation	=	5
Minimum gate overlap into field area	=	3

LAYER 5 P2.

Tolerance w.r.t drawn feature size	=	+0.75 or -0.5
Minimum rail width	=	6
Minimum length MOST gates	=	6
Minimum separation	=	5
Minimum gate overlap into field area	=	5

LAYER 6 CT.

Minimum contact size	=	6 X 6
Minimum overlap of P1 around contact hole	=	2
Minimum overlap of P1 around contact hole when overlap is crossed by aluminium	=	6
Minimum overlap of n^+ diffusion around contact hole	=	6
Minimum separation between contacts and unrelated P1	=	4
Minimum separation between contacts and unrelated P2 or AA	=	6

LAYER 8 AL.

Tolerance w.r.t drawn feature size	=	-2.25 to -0.75
Minimum rail width	=	7
Minimum separation	=	6
Minimum overlap around contacts	=	2
Minimum bond pad size	=	100 X 100
Preferred bond pad size	=	120 X 120
Minimum spacing between bond pads	=	60
Minimum separation between bond pads and unrelated aluminium	=	20

LAYER 9 PA.

Minimum clearance inside bond pads	=	6

ELECTRICAL SPECIFICATIONS.

POLYSILICON ONE MOST. ENHANCEMENT.

Extrapolated threshold, Vto	1.25 + or - 0.25 V
Zero body effect threshold, Vtoo	0.5 V
Body constant, k	$0.3\ V^{0.5}$
Gain factor, Bo	$25\ \mu A\ /\ V^2$
Gain factor reduction constant, θ	$0.05\ V^{-1}$
Threshold temperature coefficient	$-2mV\ /\ ^{o}C$
Gain factor temperature dependence	proportional to T^2

POLYSILICON TWO MOST. ENHANCEMENT.

Extrapolated threshold, Vto	3.5 + or - 1.0 V
Gain factor, Bo	$17\mu A\ /\ V^2$
Gain factor reduction constant, θ	$0.05\ V^{-1}$

POLYSILICON ONE MOST. DEPLETION.

Extrapolated threshold, Vto	-8.0 + or - 1.0 V
Gain factor, Bo	$17\mu A\ /\ V^2$

POLYSILICON TWO MOST. DEPLETION.

Extrapolated threshold, Vto	-4.0 + or - 1.0 V
Gain factor, Bo	$14\mu A\ /\ V^2$

BRIEF ELECTRICAL CHARACTERISTICS.

Breakdown voltage, BVdss	> 20 V
Spurious threshold voltage, Vt'	> 20 V

Sheet resistance.

n^+ diffusion	10 - 20 ohms/sq.
polysilicon one	20 - 50 ohms/sq.
polysilicon two	20 - 50 ohms/sq.
aluminium	0.03 ohms/sq.

Capacitance. (Only calculated values available.)

Poly one over thin oxide	3.6×10^{-4} pF/μ^2
Poly two over thin oxide	3.0×10^{-4} pF/μ^2
Poly one over field oxide	3.6×10^{-5} pF/μ^2
Poly two over field oxide	4.0×10^{-5} pF/μ^2
Poly two to Poly one	1.8×10^{-4} pF/μ^2
Aluminium to Poly one	3.3×10^{-5} pF/μ^2
Aluminium to Poly two	3.3×10^{-5} pF/μ^2
Aluminium to substrate	1.8×10^{-5} pF/μ^2
Gate to source or drain, P1	4.5×10^{-4} pF/μ^2
Gate to source or drain, P2	3.7×10^{-4} pF/μ^2
n^+ to substrate, area term	$\frac{0.7}{(V + 0.6)} \times 10^{-4}$ pF/μm^2
periphery term	$\frac{8}{(V + 0.6)} \times 10^{-4}$ pF/μm

APPENDIX D: TARGET SPECIFICATIONS AND THE CIRCUIT DIAGRAM FOR THE EXPERIMENTAL NMOS OPERATIONAL AMPLIFIER

The experimental NMOS operational amplifier employed 18 P_1-gate enhancement transistors and 6 P_2-gate depletion transistors, giving a total of 24 MOS transistors, as shown in Fig.D.1. The input capacitance was calculated to be 0.08pF and the overall layout area was 0.087 mm^2. The output voltage swing of the operational amplifier was 3.5 to 8.5 volts, limited by the fact that there are transistors within the operational amplifier from its output to both V_{DD} and V_{SS} power supply rails. These devices must remain in saturation in order for the operational amplifier to achieve its full gain. Target specifications for the NMOS operational amplifier employed in the experimental switched-capacitor lowpass ladder filter are given in Table D.1.

	MIN	TYP	MAX	UNITS
Input Capacitance		0.08		pF
Open Loop Gain	1000		9000	
Unity Gain Bandwidth		2		MHz
Output Range	3.5		8.5	Volts
Input Range	3.5		9.0	Volts
V_{DD} Supply		15		Volts
V_{BB} Supply		-5		Volts
Open Loop Output Resistance	1K5	2K	2K5	
Power Dissipation		5		mW

TABLE D.1: Target specifications for the experimental NMOS operational amplifier.

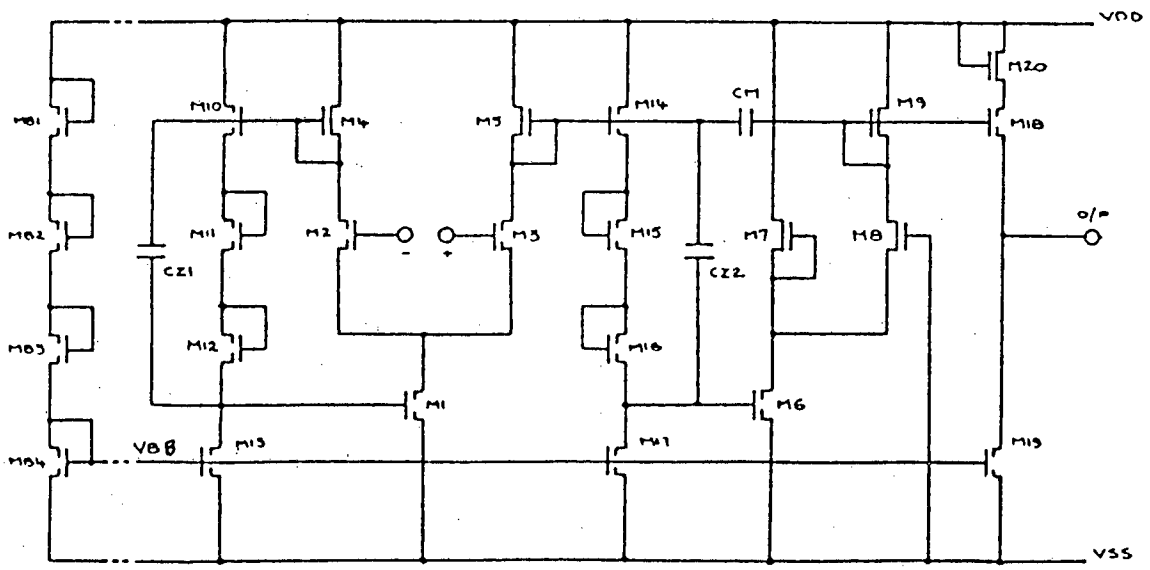


FIG.D.1: Circuit diagram for the experimental NMOS operational amplifier.

APPENDIX E: AUTHOR'S PUBLISHED WORK

EXPERIMENTAL VALIDATION OF EXACT DESIGN OF SWITCHED-CAPACITOR LADDER FILTERS

Indexing terms: Circuit design, Switched-capacitor networks

Experimental results validating a recently introduced exact theory for switched-capacitor lowpass ladder filters are presented. The prototype filter is a third-order Butterworth design using a low sampling/filter-cutoff ratio of 8·28 and has been fabricated in monolithic form.

Introduction: Switched-capacitor (SC) ladder filters are currently being widely developed for telecommunication systems, and clearly the optimum design of such filters is a major goal. The established design technique for such filters,[1,2] which employs active ladder or 'leapfrog' structures, has been based on the tacit assumption of a high clocking-rate/filter-cutoff-frequency ratio to permit simplified theory and to compensate for sampling effects, for example. This high ratio assumption, which is at the root of the switched-capacitor technique, and results from the equivalence between a resistor simulation by a 'switched-capacitor', limits the useful frequency range of the filter and increases the capacitor ratios required. This limitation therefore leads to unnecessarily large chip area to accommodate the capacitor ratios when the filters are integrated.

Recently, an exact analysis and design method based on distributed circuit theory has been introduced by Scanlan.[3] With this exact design method, switched-capacitor ladder filters are treated strictly as sampled-data filters. Thus the case of high sampling rates is dealt with as a limiting situation, rather than with the established approximate theory where the analysis is only applicable at high sampling rates.

In this letter we have designed a simple third-order Butterworth lowpass ladder filter in integrated circuit form based on the exact theory[3] to validate its applicability at low clock rates. This simple filter example can be treated analytically without the use of involved computer routines, and therefore helps to illustrate the efficacy of the exact analysis at low clocking rates.

Design comparison: Exact analysis of SC lowpass filters[3] indicates that their equivalent *RLC* ladder filters do not have frequency-independent termination resistors. This contrasts with the assumption made in approximate designs where the termination resistors are assumed to be frequency independent. Therefore, a different approach to the development of an analysis should be employed in determining the optimum element values.

A recently introduced exact design method[3] utilises a suitable transfer function for the synthesis of SC ladder filters. This transfer function, which has equiripple and maximally flat solution, is the transfer function of n cascaded unit elements. In the maximally flat case, this leads to

$$|H_{21}|^2 = \frac{K}{1 + \left(\dfrac{\sin\theta}{\sin\theta_0}\right)^{2n}} \quad (1)$$

In the simple example we have used, $n = 3$, $K = 0{\cdot}25$, $\theta_0 = \pi(\omega_0/\omega_s) = \pi(1/8{\cdot}28)$ where ω_0 and ω_s are the passband edge and sampling frequencies, respectively, or, alternatively, the cutoff frequency of the lowpass filter example is 12% of the clock frequency. For our example, the transfer function takes the form

$$|H_{21}|^2 = \frac{0{\cdot}25}{1 + 334\sin^6\theta} \quad (2)$$

but, using the established approximate design[1,2] element values, it will be given by

$$|H_{21}|^2 = \frac{0{\cdot}25}{1 - \sin^2\theta + 246\sin^6\theta} \quad (3)$$

Comparison of eqn. 3 with the exact relationship given by eqn. 2 shows clearly that the filter will have a distorted response if the approximate analysis is adopted.

In Fig. 1 we give the frequency responses for the approximate analysis (curve *a*) and the exact analysis (curve *b*), which is by definition the Butterworth design curve. In this example the filter cutoff frequency is 12% of the clock frequency. By using lower percentage ratios (3–4%), which are more usual for existing SC filter designs, for approximate design, the results for the exact and approximate theories are closer. However, as Table 1 indicates, the exact analysis requires lower capacitor ratios here which in turn leads to more compact circuit topology.

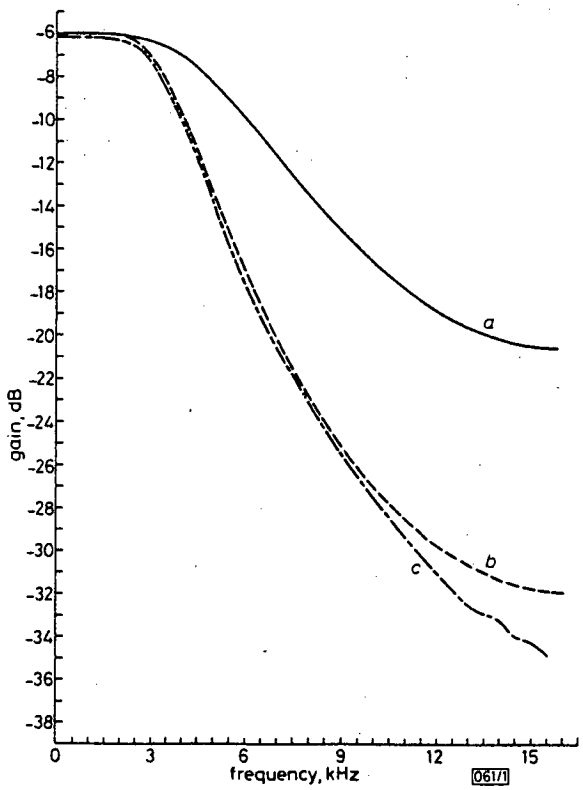


Fig. 1 *Response of switched-capacitor lowpass ladder filter*
- *a* Calculated frequency response based on approximate design method
- *b* Calculated frequency response based on exact design method
- *c* Measured frequency response of filter based on the exact design method (for clock frequency of 32 kHz)

Table 1 REQUIRED CAPACITOR RATIOS

See Fig. 2	1st stage	2nd stage	3rd stage
Approximate design*[1,2]	4·77	9·55	4·77
Exact design[3]	2·90	2·40	1·50

* Example: clock frequency needs to be at least 4 times larger than for exact design

Experimental results: A prototype integrated SC filter based on the simple lowpass example and using the capacitor ratios given in Table 1 (exact design) was realised in a 6 μm 15 V polysilicon-gate NMOS process. The experimental curve for a typical filter is given in Fig. 1*c*. Excellent agreement between the exact theory and experiment is evident. The deficiency of the approximate analysis is also clearly seen and, according to Table 1, would require an increase of capacitor ratios and clocking frequency to approach the exact curve.

Conclusions: This letter confirms that the exact theory of SC ladder filter designs must be applied at low sampling rates relative to the clocking frequency, in preference to the approximate design approach. Even at high sampling rates, where the approximate analysis gives acceptable results, use of the exact theory leads to optimum element values.

Reprinted from ELECTRONICS LETTERS 2nd April 1981 Vol.17 No.7 pp.275-276

The advantage gained by the adoption of the exact design approach is that for high cutoff frequency filters the clocking rate may be lower. This has useful implications in that in addition to the lower capacitor ratios, the clock generator design can be simpler and the power should be lower. On the other hand, for filtering requirements where a higher clock frequency can be used, the simple approximate theory leads to, usually adequate, nonoptimised designs and the specification of the inevitable antialiasing filter is relaxed.

Trade-offs between the sampling rate, passband ripple, maximum attenuation, dynamic range and filter layout area in integrated form are all factors which must be taken into consideration in comparing the alternative design approaches. This aspect is the subject of future work.

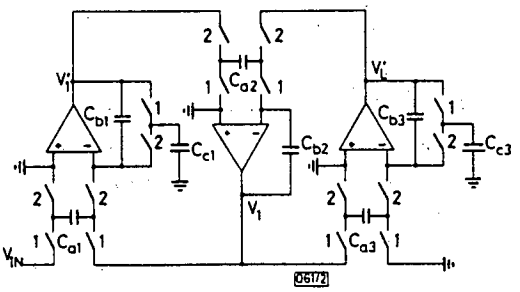


Fig. 2 *Switched-capacitor lowpass ladder filter*

Acknowledgments: The authors acknowledge the support of the Science Research Council. The first author would like to acknowledge the financial support of the University of Baluchistan, Zahedan, Iran. This research has been undertaken in collaboration with Prof. J. O. Scanlan of University College, Dublin.

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